A 0.55V Bandgap reference with a 59ppm/^{0}c Temperature coefficient

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This paper presents a novel low power, low voltage CMOS bandgap reference (BGR) that overcomes the problems with existing BJT-based reference circuits, by using a MOS transistor operating in sub-threshold region. A proportional to absolute temperature (PTAT) voltage is generated by exploiting the self-bias cascode branch, while a Complementary to Absolute Temperature (CTAT) voltage is generated by using the threshold voltage of the transistor. The proposed circuit is implemented in 65nm CMOS technology. Post-layout simulation results show that the proposed circuit works with a supply voltage of 0.55V, and generates a 286mV reference voltage with a temperature coefficient of 59ppm/°C. The circuit takes 413nA current from 0.55V supply and occupies 0.00986mm^2 of active area.

Keywords— Low Power, Low Voltage PTAT, CTAT

1. Introduction

Many applications, such as wearable electronics, bio-medical analog systems and wireless sensor nodes, requires a voltage reference circuit that is independent of process, voltage, temperature (PVT) and corner variations. Typically the well known bandgap reference circuit (BGR) suits this purpose [2]. In a bio-medical transceiver, the ADC plays a major role in determining the sensitivity of the entire link, and its own resolution depends on the effective number of bits (ENOB), which in turn is affected by the accuracy of the reference voltage. Apart from performance, the power dissipation of these circuits becomes an issue due to the battery life time concerns regarding implantable medical devices. Therefore, the design of high precision voltage/current reference circuits with ultra-low-power dissipation has become a priority. Another challenge in the design of these analog precision circuits for bio-medical transceivers is the low power supply requirement (<0.6V), since they are often implemented in deep submicron CMOS technology nodes to enable them with digital signal processing capabilities. [1]

Since the first BJT-based bandgap reference design was introduced [2], it has been improved continuously in many aspects to minimize the power dissipation, reduce the operating voltage and improving robustness against startup issues. The current trend however is to design the BGR with pure CMOS, without the need of any parasitic prone BJTs. In light of that, this paper presents a novel ultra-low power, low voltage bandgap design utilizing only MOS transistors. After this introduction, the rest of the paper has been organized as follows: Section-2 serves as a literature survey of the existing BGRs and their principle of operation, Section-3 explains the proposed circuit concept and section-4 presents the simulation results.

2. review of existing bandgap reference circuits

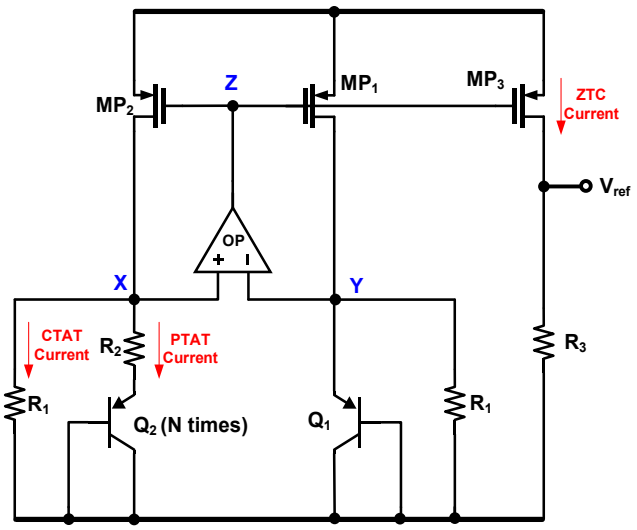

Fig. 1. Conventional Sub-1V CMOS bandgap reference **[3]** (Without start-up circuit)

The base to emitter voltage (V_{BE}) of a BJT can be expressed as follows:

$$V_{BE}(T) = V_T \ln\left(1 + \frac{I_C}{I_S}\right) \tag{1}$$

Where I_C is the bias current and I_S is the reverse saturation current.

Equation (1) reveals that it has a negative temperature coefficient due to the temperature dependency of I_S, hence this acts as CTAT. If two BJTs operate at different current densities, the difference of their V_{BE}'s presents an excellent PTAT, which can be expressed as follows:

$$V_{BE1} - V_{BE2} = V_T ln(n) \tag{2}$$

The principle of a bandgap reference circuit is the use of a weighted summation of the Proportional to Absolute Temperature (PTAT) voltage and the Complimentary to absolute Temperature (CTAT) voltage in such a way that yields the minimum dependence on temperature. This was originally proposed by Brokaw [2] for a higher output voltage with pure BJTs to make it CMOS compatible and reduce the mask cost. Implementations based on the vertical parasitic PNP transistors available in the NWELL were utilized. Almost

every architecture in the literature using the V_{BE} of the BJT as the CTAT (due to the reverse saturation current sensitivity) and difference between the V_{BE} of the scaled BJT's as the PTAT. This architecture can only output 1.26V at room temperature, hence it requires a relatively high power supply voltage. Fig.1 shows a conventional sub-1V bandgap [3]. It modifies the Brokaw BGR [2] by adding parallel resistors to the two BJTs. The current through R_2 (I_{R2}) has a PTAT nature due to the voltage across it, whereas the current through R_1 (I_{R1}) has CTAT nature because node X potential is CTAT in nature. These two currents can be expressed as follows:

$$I_{R2} = \frac{V_T \ln(n)}{R_2} \quad \text{and} \quad I_{R1} = \frac{V_{BE}}{R_1} \tag{3}$$

By adding these two currents with appropriate weights, a zero-temperature coefficient (ZTC) reference current can be obtained, which will produce bandgap voltage across R_3.

$$V_{REF} = \left(\frac{V_T \ln n}{R_2} + \frac{V_{BE}}{R_1}\right) R_3 \tag{4}$$

To render ZTC, $\frac{R_2}{R_1} * \ln n$ is chosen as ~17.2 provided the slope of V_{BE} is -2mv/^{0}C. This architecture can support a much lower voltage than the conventional Bandgap [2] by carefully setting the R3 value, because this value doesn't change the ZTC operation. In general, BJT-based BGR, including the one in Fig.1, suffers from the following problems:

1) The circuit dissipates a lot of power because a BJT needs to be biased with a current much higher than the reverse saturation current. Fig. 2 shows the slope of the PTAT with the temperature for different bias currents and reveals that a constant slope is only obtained when the bias current is greater than 0.9uA. When the bias-current is lower than this, the PTAT slope deviates from the nominal value.

2) In a typical process V_{BE} of the BJT is ~700mV, but at higher temperatures this can be as high as 820mV (due to its negative temperature coefficient), hence limiting the minimum supply requirement of the circuit [4]. In the deep submicron CMOS technologies such as 65nm, the vertical parasitic PNP current gain (β) is not more than 3, which will create non PTAT errors due to the base resistance voltage drop.

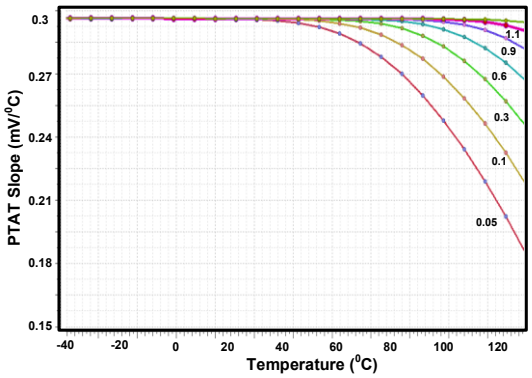

Fig. 2. Proposed bangap reference circuit

To combat the problem described above and make it suitable for ultra-low power applications without requiring any special devices, several MOS only BGRs implementations have been introduced [5-8]. To understand their advantage in comparison to BJT-based implementations, one has to understand that the main difference between BJT and MOS reference circuits is that the former relies on the energy bandgap of the silicon (E_G~1.2eV). The latter depends on a threshold voltage (V_{th}~0.3V), hence MOS-only-BGR can work with much less current and voltage. In-fact both BJT and MOS sub-threshold current equations shows exponential dependency as expressed below:

$$I_{BJT} = I_o e^{\frac{-V_{ds}}{V_T}} \left(e^{\frac{V_D}{nV}} - 1 \right) \tag{5}$$

$$I_{MOS} = \frac{W}{L} I_0 exp\left(\frac{V_{gs}-V_{th}}{\eta V_T}\right)\left(1 - exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{6}$$

Where $I_o = \mu_n C_{ox}(\eta - 1)V_T^2$, and W is the width is the length, $\mu_n$is electron mobility, $C_{ox}$is gate oxide capacitance, η is sub-threshold slope factor, V_T is thermal voltage, and $V_{th}$is the threshold voltage.

The implementations [5-8] rely on the fact that V_{GS} of the MOS transistor decreases with temperature, hence it is a CTAT, and the difference in the V_{GS} of two transistors is PTAT. These implementations however, show significant power supply sensitivity and use higher power, though their power dissipations in general is still much less than BJT-based implementations.

3. proposed bandgap reference.

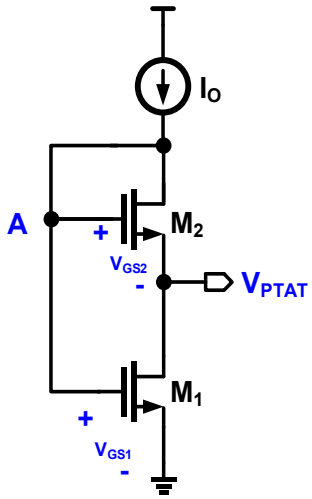

Fig. 3. PTAT Genearator

Fig. 3 shows the PTAT generator used in the majority of CMOS only based reference circuits [8]. This is a well-known circuit used to generate bias for Cascode circuits when they are operating in saturation region, but in the present scenario devices must be in the sub-threshold region for the exponential I-V relation. From Fig. 3, the output voltage V_{PTAT} can be written as $V_{PTAT} = V_{GS1} - V_{GS2}$. When $V_{DS}>4V_T$ of the sub-threshold biased device and the v_{ds} term in the equation (6) can be neglected, hence, the equation can be re-written as follows:

$$I_D = \frac{W}{L} I_0 exp\left(\frac{V_{gs}-V_{th}}{\eta V_T}\right) \text{ and } V_{gs} = V_{th} + \eta V_T \ln\left(\frac{I_d}{\frac{W}{L}I_0}\right) \tag{7}$$

From the above equation: V_{GS} depends on the current density of the device, so making M_2 λ times larger than M_1 will generate PTAT as expressed in the following.

$$V_{gs1} = V_{th} + \eta V_T \ln\left(\frac{I_d}{\frac{W}{L}I_0}\right) \quad \text{and } V_{gs2} = V_{th} + \eta V_T \ln\left(\frac{I_d}{\lambda\frac{W}{L}I_0}\right) \tag{8}$$

$$V_{PTAT} = \eta V_T \ln(\lambda) \text{ where } \lambda = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \tag{9}$$

The threshold voltage of the MOS transistor will decrease with temperature, because increasing temperature will increase the carrier thermal energy, hence requiring less voltage at the gate to form the inversion layer. This can be approximated to a first order polynomial expression as follows [9] where K_{th} is the temperature coefficient of V_{gs}~-0.3mv/^{0}C

$$V_{gs}(T) \sim V_{gs}(T_0) + K_{th}\left(\frac{T}{T_o} - 1\right) \quad (10)$$

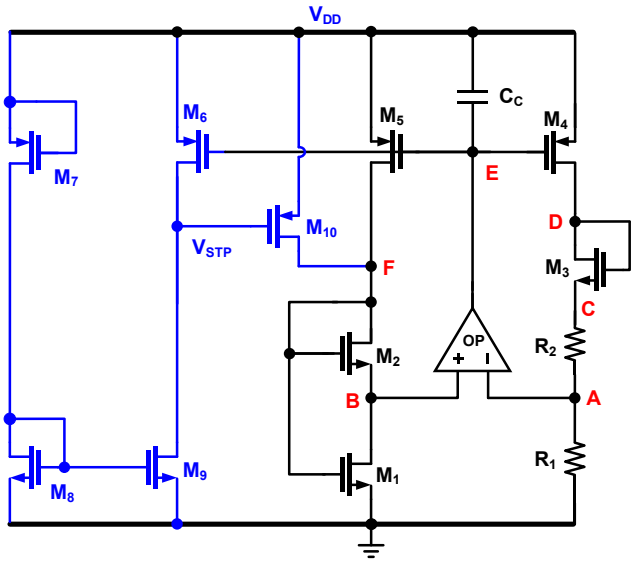

Fig. 4. Proposed Bandgap reference circuit.

Fig. 4 depicts the proposed bandgap circuit. As explained in the previous section, node B voltage has a PTAT nature. Due to the negative feedback nature, the opamp maintains a very low input offset, hence node A potential is also of a PTAT nature [10][11]. The voltage across resistor R_1 is also of PTAT nature, hence all transistors in the core circuit carry a PTAT current. Similar to a BJT-based BGR, this circuit also must generate a scaled sum of V_{GS} and ΔV_{GS} to produce a ZTC voltage reference. Since R_1, R_2 are in series, Node C potential is an amplified version of the PTAT.

$$I_{R1} = \frac{\eta V_T \ln(\lambda)}{R_1} \quad (11)$$

$$V_C = \eta V_T \ln(\lambda)\left(1 + \frac{R_2}{R_1}\right) \quad (12)$$

To add PTAT voltage to CTAT voltage, a diode-connected large aspect ratio transistor (M_3) is connected in series, as shown in Fig. 4. The reference voltage will be generated at node-D. The reference voltage can be expressed as:

$$V_{REF} = V_{GS3} + \eta V_T \ln(\lambda)\left(1 + \frac{R_2}{R_1}\right) \quad (13)$$

To minimize the temperature coefficient of the reference voltage, differentiating equation (13) and equating it to zero would give the PTAT scaling factor:

$$\frac{\partial V_{\text{ref}}}{\partial T} = \frac{\partial V_{gs3}}{\partial T} + \eta \frac{\partial V_T}{\partial T} \ln(\lambda) \left(1 + \frac{R_2}{R_1}\right) = 0 \tag{14}$$

$$\frac{R_2}{R_1} = \frac{-\frac{\partial V_{gs3}}{\partial T}}{\eta \frac{\partial V_T}{\partial T} \ln(\lambda)} - 1 \tag{15}$$

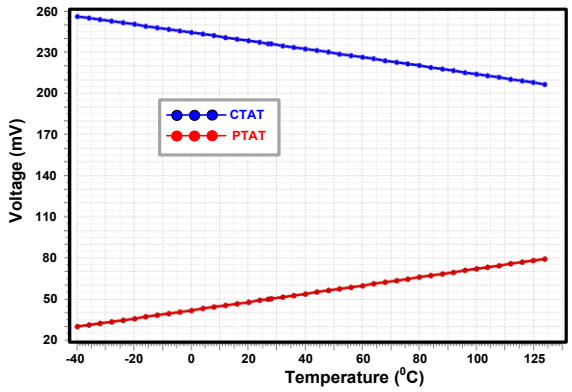

Fig. 5. Simulated CTAT and PTAT voltages.

The ratio of resistors will be decided by (15) to achieve a minimum temperature coefficient, from the equation it only depends on temp coefficient of V_{GS3}, V_T, and λ. The former two parameters are technology dependent parameters and the later parameter λ (ratio of transistors) is the only free variable that can be chosen whilst designing, however, this will affect the design in many aspects. The smaller the ratio, the larger the PTAT gain (R_2/R_1) to minimize the temp-coefficient. Equation (13) assumes an ideal opamp without having any input referred offset, by conserving output voltage can be expressed as follows:

$$V_{REF} = V_{GS3} + \eta V_T \ln(\lambda) \left(1 + \frac{R_2}{R_1}\right) + V_{OS} \left(1 + \frac{R_2}{R_1}\right) \tag{16}$$

The offset (V_{os}) is also amplified by the PTAT gain, so it is very important to minimize the resistor ratio, hence the transistor ratio also needs to be maximized, but very high values of λ will create mismatch problems in the transistors. To balance both effects, a ratio of 24 has been chosen. By substituting the numerical values into the equation (15), we can obtain a resistor ratio of 0.0808. Whilst maintaining this resistor ratio, R_1 value must be maximized to minimize the power, because V_{PTAT}/R_1 dictates the bandgap core dc bias current. To minimize the temperature coefficient, resistor values R2 and R1, in (15), are chosen to be 80KΩ and 990KΩ respectively. Fig. 5 shows the simulation results of the PTAT and CTAT voltages with the above specified component values and transistors ratio. As with any reference circuit, the proposed circuit also needs a start-up circuit to kick the

circuit out of un-desirable zero current operating points. M_7,M_8 form a small fixed current leg and M_6,M_9 copy the current from the bandgap core. The V_{STP} node indicates the bandgap current level and transistor M_{10} pumps current into the circuit to avoid the startup problem. A conventional two stage Miller compensated opamp with a PMOS input stage has been used to enable negative feedback. The opamp has 60^0 phase margin and 12dB gain margin for a good step response [12].

4. Simulation results

The proposed bandgap reference circuit was implemented in 65nm CMOS technology, and post-layout simulations were carried out. Fig. 6 shows how the reference varies across the industrial temperature range (-40-125^{0}C) for different PVT corners. The nominal reference voltage is ~287mV and 2.8mV is the max variation over the temperature range and 1.2mV over the process corners. Hence the temperature sensitivity is 59ppm/^{0}C.

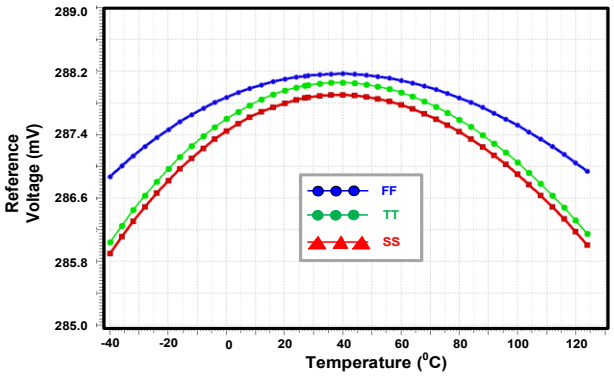

Fig. 6. Simulated Reference voltage with temperature.

Fig. 7 shows the Monte-Carlo variation of the output voltage, to estimate the batch to batch variation in the real-time production. A 400-point simulation shows that output voltage has an average of 286mV and 3.2mV of the standard deviation, means 3.3% of variation. Hence 99.97% of the fabricated chips will results in 3.3% variation in the mean output voltage. Fig. 8 shows how the output voltage varies with respect to the supply voltage. From the plot, it is evident that the circuits work with minimum voltage of 550mV. Increasing the supply voltage to 800mV results in 6.5mV variation in the output voltage.

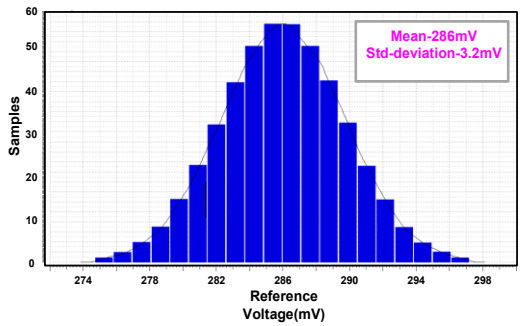

Fig. 7. Monte Carlo variation.

When the supply drops below 500mV, the reference voltage decreases significantly because the Opamp is not working in high gain mode and the bandgap core devices are not getting sufficient V_{ds} to keep the current constant. Fig. 9 shows the simulated noise at the output of the reference circuit. Spot noise at 1MHz is 10^{-15} V^2/Hz and integrated noise in the frequency of interst is 3.98µV. The noise level achieved is more than sufficient for bio-medical transcivers circuits, such as 8-bit ADC and Variable Gain amplifier(VGA) bias circuits[7].

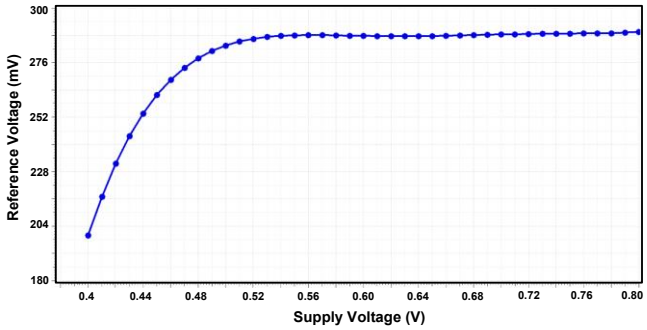

Fig. 8. Simulated output voltage sensetivity with Supply Voltage.

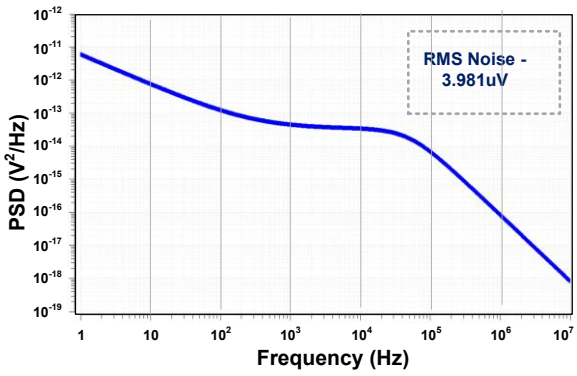

Fig. 9. Simulated Noise at 120^0 Temperature..

Fig. 10 shows the layout of the proposed circuit. The active area is 68*145um^2. Care has been taken to minimize the STI well proximity effects by keeping the PMOS devices far from the n-well and adding enough dummy devices on both sides of the active area [13].

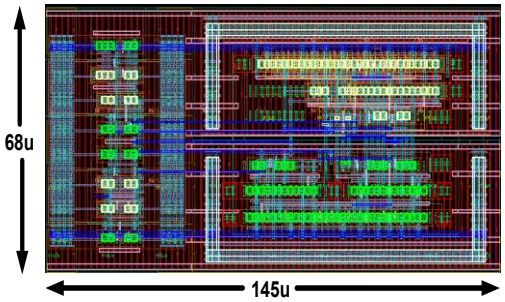

Fig. 10. Layout of bandgap reference.

Table-1 SUMMARIZES the performance of the bandgap circuit.

Table-1 Performance summary

Parameter	**Result**	**Unit**
Output Voltage	286	mV
Power supply	0.55	V
Temperature range	-40-125	^{0}C
PSRR @1MHz	-70	dB
Integrated Noise(10KHz-15MHz)	3.981	uV
Temperature Coefficient	59	ppm/^{0}C
Line Sensitivity	2.56	%
Power Consumption	0.2271	uW
Technology	65	nm
Area	0.009862	mm^2

5. Conclusion

In this paper, a compact nanowatt CMOS bandgap reference utilizing only MOS transistors has been presented. The bandgap has been implemented in low voltage, deep sub micro technologies. It is suitable for wearable applications, where battery life is of primary importance.

6. References

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