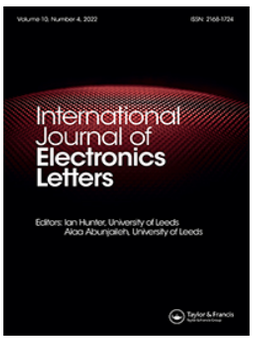

International Journal of Electronics Letters

ISSN: (Print) (Online) Journal homepage: https://www.tandfonline.com/loi/tetl20

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**To cite this article:** R. Nagulapalli, N. Yassine, S. Barker, P Georgiou & K. Hayatleh (2022) A 261mV Bandgap reference based on Beta Multiplier with 64ppm/0C temp coefficient, International Journal of Electronics Letters, 10:4, 403-413, DOI: 10.1080/21681724.2021.1966656

**To link to this article:** https://doi.org/10.1080/21681724.2021.1966656

INTERNATIONAL JOURNAL OF ELECTRONICS LETTERS
2022, VOL. 10, NO. 4, 403–413
https://doi.org/10.1080/21681724.2021.1966656



# A 261mV Bandgap reference based on Beta Multiplier with 64ppm/0C temp coefficient

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**ABSTRACT**

In this paper, a low voltage bandgap reference circuit has been proposed. The introduction of a modified beta multiplier bias circuit decreased the mismatch caused by the PMOS transistors opamp contribution. By shifting the fixed resistors to the NMOSs drain side, the beta multiplier bias minimised threshold mismatch between the two NMOS transistors. A 200-point MC simulation showed a 0.9 mV standard deviation, with a 0.34% accuracy. The simulated temperature coefficient was 64 ppm/$^0$C. The proposed circuit consumed 5.04 µW of power from a 0.45 V power supply voltage. A prototype was implemented in 65 nm CMOS technology occupying a 2888 µm$^2$ silicon area, with the nominal value of the reference at 261 mV.

**ARTICLE HISTORY**
Received 4 November 2020
Accepted 28 July 2021

**KEYWORDS**
BGR; noise; phase margin; OTA; PSRR; CTAT

## 1. Introduction

The bandgap reference (BGR) is a critical circuit in analogue, mixed-signal, radiofrequency and biomedical applications. It provides temperature-independent voltage/current to reference a Low Dropout Regulator (LDO) or biasing voltage of critical circuits. Its output voltage should also be much less sensitive to Process Voltage and Temperature (PVT) corners (Wong et al., 2004). Meanwhile, it needs to be ultra-low power for biomedical devices that operate on battery power; hence, battery life is significant. Low-temperature drift circuits are critical analogue block in wearable biomedical devices. For instance, an ADC with a 1 mV resolution requires a BGR circuit with 0.5 mV worst-case temperature drift (Nagulapalli et al., 2017). Hence, this shows the necessity of a highly accurate reference circuit.

The required temp coefficient is approximately 100 ppm, which is very challenging at sub-1 V without consuming too much power. Hence, there is a clear motivation to explore minimal temperature coefficient BGR architecture with lower operating supply voltage.

The fundamental principle of the BGR circuit is as follows. A scaled version of Complimentary to Absolute Temperature (CTAT) and Proportional to Absolute Temperature (PTAT) would need to cancel out their respective temperature coefficients to minimise the temperature coefficient. Hence, this would make the output voltage independent of the temperature. There are initial proposals based on Bipolar Junction

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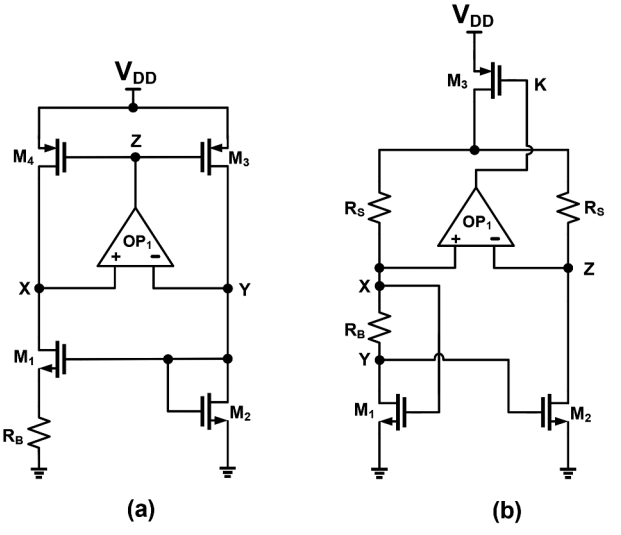


Figure 1. (a) Conventional. (b) Proposed beta multiplier.

Transistors (BJT) (Banba et al., 1999; Tsividis & Ulmer, 1978). However, due to the large area and fabrication requirements of BJTs, MOS-based reference circuits have become very popular. This paper proposes an only MOS-based bandgap reference. The rest of the paper is organised as follows: Section-2 explains the principle of the beta multiplier, Section-3 describes the proposed low voltage technique, and finally, Section-4 summarises the simulation results of the prototype and provides a comparison with the existing solutions.

## 2. Proposed beta-multiplier

The Beta Multiplier self-bias circuit was proposed originally in (Liu & Baker, 1998) to get the constant $g_m$ of a transistor due to the PTAT current. Figure 1(a) shows the conventional circuit, where $M_1$ is four times greater in size than $M_2$, such that the overdrive voltage of $M_2$ is two times higher than $M_1$. The currents through these two transistors are equal due to the formation of a PMOS current mirror by transistors $M_3$, $M_4$ and a bias opamp. It has negative and positive feedback, with the negative feedback going through the degeneration resistance ($R_B$) and positive feedback through $M_1$, $M_2$, $M_3$ and $M_4$. All the transistors are biased in the saturation region.

The voltage across the resistor ($R_B$) is the difference between the two transistors gate-to-source voltages, and mathematically we can show that $g_{m2}$ is only dependent on $R_B$. Let us say that $V_{gs}$ is the gate to source voltage, and $V_{th}$ is the threshold voltage of the transistor.

$$V_{gs2} - V_{th} = 2\left(V_{gs1} - V_{th}\right) \tag{1}$$

$$V_{gs2} - V_{gs1} = I_B R_B \tag{2}$$

From (1) & (2), we can derive the overdrive voltage of $M_2$ as follows.

$$V_{gs2} - V_{th} = 2I_B R_B \tag{3}$$

The expression of the transconductance of transistor $M_2$ ($g_{m2}$) is as follows.

$g_{m2} = \frac{2I_B}{V_{gs2} - V_{th}} = \frac{1}{R_B}$ (4)

Additionally, the expression of the current through $M_2$ is as follows (it reveals that it is independent of supply voltage).

$$I_B = \frac{1}{2\mu_n C_{ox} \frac{W}{L} R_B^2} \tag{5}$$

Though this circuit stabilises the $g_m$ very well, it has a few downsides. While deriving Equation (3), it was assumed that the threshold voltage of $M_2$ and $M_1$ are equal ($V_{th2} = V_{th1}$). However, unfortunately, this is not a very valid assumption since the $M_1$ source potential is higher than the ground potential by $I_B R_B$. Whereas the source potential of $M_2$ is at ground potential. Hence, due to the body effect, $V_{th1}$ is slightly higher than $V_{th2}$, contributing to significant error in the currents in $M_1$, $M_2$ and $g_{m2}$. The error is significant, especially in deep sub-micron CMOS technologies where the body effect is large.

The mismatch results in the bias circuit are due to the current mirror mismatch formed by $M_3$, $M_4$, and the opamp offset (Navarro & Ishibe, 2011). We have proposed a modified beta multiplier to solve these problems, as shown in Figure 1(b). PMOS current sources were replaced by a pair of resistors, with the current through them adjusted by the opamp and transistor $M_3$. This way, the mismatch introduced by PMOS transistors were significantly reduced due to the resistors matching very well, compared to the MOS transistors (Perry et al., 2007). $M_1$ and $M_2$ sources are grounded to solve the body effect problem, but a voltage difference across the resistor created the drain, as shown in Figure 1(b). Node x, y voltages are the transistor gate to source voltages ($V_{gs}$) of $M_1$ and $M_2$. The voltage drop across $R_B$ is the difference between $V_{GS1}$ and $V_{GS2}$. The proposed circuit works similarly to the conventional ones regarding stabilising the $g_m$ but with improved mismatch characteristics.

## 3. Proposed technique

Several MOS transistor-based reference circuits have been proposed. In (Navarro & Ishibe, 2011), a current-mode circuit is proposed, where separate CTAT and PTAT currents have been generated. Almost all the references generate PTAT and CTAT with the same principle, but implementing the final summation and output generation is what makes the difference. This circuit could run with 500 mV supply voltage, but the accuracy was poor due to multiple branches. (Perry et al., 2007) proposed a high accurate reference by feeding error signals into the BJT base. However, this circuit requires a 1.4 V supply. (Shetler et al., 2015) describes a radiation hardening reference circuit, which uses resistors instead of PMOS current sources to define the core current. Unfortunately, this circuit requires a 1.8 V supply. The following thought process has been carried out to develop a highly accurate circuit that runs on less Vdd. In general, the transistor gate to source voltage ($V_{gs}$) and threshold voltage ($V_{th}$) decreases with temperature. An increase in temperature increases the electron thermal energy and therefore requires less voltage to invert the channel in the MOSFET. Hence (7) shows the first-order polynomial with a negative slope approximated (Wang et al., 2016).

$$V_{gs}(T)\ V_{gs}(T_0) + K_{th}\left(\frac{T}{T_o} - 1\right) \tag{7}$$

Where $K_{th}$ is the temperature coefficient of $V_{gs}$.

Figure 2 shows the simulated gate to source voltage of the transistor with respect to temperature and shows a CTAT nature with a − 0.29 mV/$^0$C temp coefficient. The drain current of the NMOS operating in the sub-threshold region can be expressed as follows.

$$I_D = \frac{}{L} I_0 exp\left(\frac{V_{gs} - V_{th}}{\eta V_T}\right)\left(1 - exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{8}$$

Where $I_o = \mu_n C_{ox}(\eta - 1)V_T^2$, W is the width, L is the length, $\mu_n$is electron mobility, $C_{ox}$ is gate oxide capacitance, $\eta$ is sub-threshold slope factor, $V_T$ is thermal voltage and $V_{th}$ is the threshold voltage. When $V_{ds} > 4V_T$ (approximately 100 mV at room temperature), the $exp\left(\frac{-V_{ds}}{V_T}\right)$ term in Equation (8) is less than 1. Also, $I_d$ is almost independent of $V_{ds}$ and is expressed in Equation (9).

$$I_D = \frac{W}{L} I_0 exp\left(\frac{V_{gs} - V_{th}}{\eta V_T}\right) \tag{9}$$

$$V_{gs} = V_{th} + \eta V_T \ln\left(\frac{I_d}{\frac{W}{L} I_0}\right) \tag{10}$$

Synthesising a low voltage BGR circuit requires two voltages in a circuit with CTAT and PTAT characteristics (Nagulapalli, Hayatleh, Barker, Tammam et al., 2018). The proposed Beta Multiplier is one way to synthesise these two voltages. Figure 1(b) shows that the node X voltage can be used as a CTAT voltage because it represents the $V_{GS}$. There is a need to keep the device dimensions so large that the overdrive voltage is much less, ensuring that $V_{GS}$ is the same as $V_{TH}$.

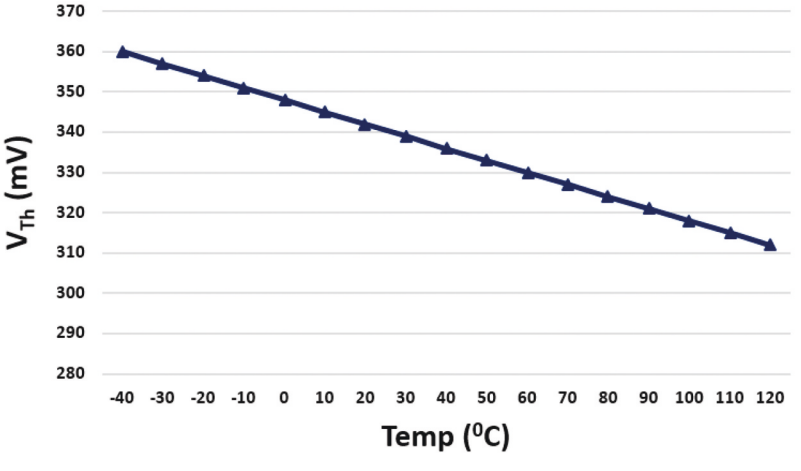


Figure 2. Temperature sensitivity of gate to source voltage (VGS).

$$V_Y = V_{GS2} = V_{th} + \eta V_T \ln \left[ \frac{\frac{I_D}{I_O}}{\frac{W_2}{L_2}} \right] \tag{11}$$

$$V_X = V_{GS1} = V_{th} + \eta V_T \ln \left[ \frac{\frac{I_D}{I_O}}{\frac{W_1}{L_1}} \right] \tag{12}$$

The voltage across the resistor can be expressed as (13), which shows very good PTAT properties that only depend on the aspect ratios of $M_1$ and $M_2$.

$$V_{RB} = V_{GS1} - V_{GS2} = \eta V_T \ln \left[ \frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}} \right] \tag{13}$$

$V_{RB}$ and $V_y$ show PTAT nature; hence both are viable in the beta multiplier bias network. A voltage summation network needs to add the scaled version of these two voltages more simply without introducing complicated noisy elements, such as opamps, to develop the bandgap reference circuit. (Wattanapanitch et al., 2007) used an opamp based V2I converter for current summation and generated unacceptable noise while performing the final addition. Figure 3 shows the proposed beta multiplier based BGR circuit with a passive summation network. A simple potential divider formed by $R_1$&$R_2$ will provide voltage summation with flexible scaling ratios. Unfortunately, the potential divider needs both voltages referenced regarding ground potential, or both need the same, non-grounded reference point (Lee, 1998). Here the CTAT voltage is with respect to the ground potential, whereas the voltage across $R_B$ is floating. Hence, it needs to be converted with reference to ground potential. As shown in Figure 4, $M_3$ carries twice the

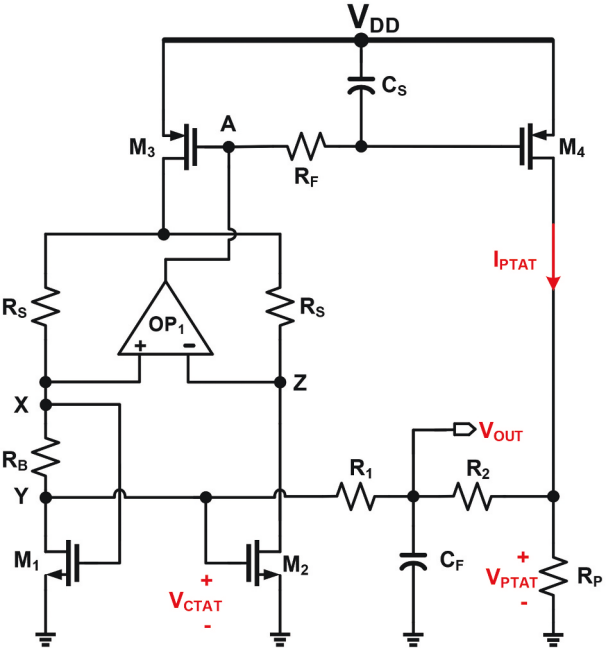


Figure 3. Proposed bandgap reference circuit.

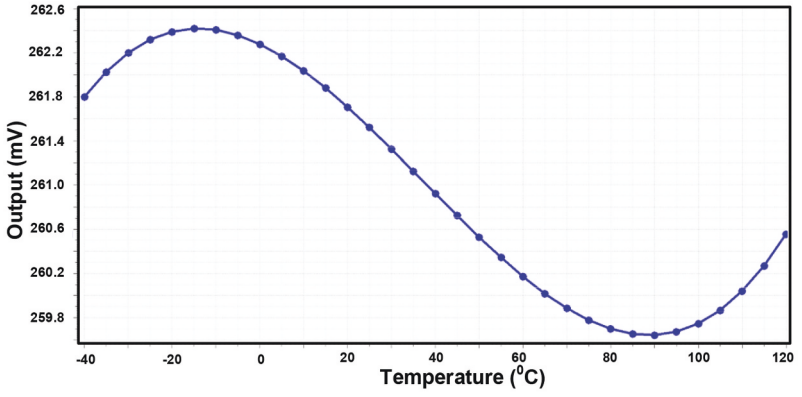


Figure 4. Temperature sensitivity of the BGR circuit.

$R_B$ current, and this current can be pumped into $R_P$ through $M_4$. (14) and (15) show how to express the current through $R_B$ and the voltage across Rp, where λ is the M1, M2 aspect ratio.

Hence, the output voltage can be expressed, as shown in (16)

(17) shows how to minimise the temperature coefficient of the output voltage, $\frac{\partial V_{ref}}{\partial T} = 0$ at room temperature.

$$I_{RB} = \frac{\eta V_T \ln[\lambda]}{R_B} \tag{14}$$

$$V_{PTAT} = \eta V_T \ln[\lambda] \frac{R_P}{R_B} \tag{15}$$

$$V_{out} = \frac{R_2}{R_2 + R_2} V_{CTAT} + \frac{R_1}{R_2 + R_2} V_{PTAT}$$

$$V_{out} = \frac{R_2}{R_2 + R_2} \left[ V_{gs2} + \eta V_T \ln[\lambda] \frac{R_P}{R_B} \frac{R_1}{R_2} \right] \tag{16}$$

$$\frac{\partial V_{\text{ref}}}{\partial T} = \frac{\partial V_{\text{gs2}}}{\partial T} + \ln[\lambda] \frac{R_P}{R_B} \frac{R_1}{R_2} \eta \frac{\partial V_{\text{T}}}{\partial T} = 0 \tag{17}$$

From Figure 2, it is clear that $\frac{\partial V_{gs2}}{\partial T} = -0.28 mV/^0\text{C}$ (at room temperature) and $\frac{\partial V_T}{\partial T} = 0.087 mV/^0\text{C}$. By substituting these values into (17), we can deduce the following.

$$\ln[\lambda] \frac{R_P}{R_B} \frac{R_1}{R_2} \eta = 3.2183 \tag{18}$$

Minimising the systematic offset requires a very high gain generated via the opamp feedback loop formed by $OP_1$, $M_3$ and $R_s$ (Leung & Mok, 2003; Nagulapalli, Hayatleh, Barker, Zourob et al., 2018). Apart from obtaining high gain with stable loop dynamics, the self-bias in the opamp could give the best results by utilising device mismatch. Hence a low voltage self-bias folded cascode opamp has been designed, where input common-

mode voltage is very low (~50-100 mV). The opamp tail current transistor is biased from node A (Figure 3) to implement self-biasing while avoiding the external opamp bias requirement. Whenever the temperature changes, the bias current in the bandgap increases due to it being proportional to absolute temperature (Shrivastava et al., 2015). Hence, if the opamp is biased with a fixed bias current, there will be a systematic offset. Fortunately, the self-bias technique tracks the opamp current with the temperature (Hamouda et al., 2013).

## 4. Prototype and simulation results

To demonstrate the robustness of the design, the circuit in Figure 3 has been implemented in 65 nm standard 1-Poly,8-Metal CMOS technology. To satisfy the zero-temperature coefficient condition (18), the values of the following poly-resistors (minimal temp coefficient) have been chosen. $R_1 = 25M\Omega$, $R_2 = 25M\Omega$, $R_P = 900K\Omega$, $R_B = 888K\Omega$ and $R_S = 24K\Omega$. At room temperature, the current flowing through the circuit is 0.25 µA. Figure 4 shows the BGR output sensitivity to the temperature; the output voltage has been changed by 2.7 mV while temperature varies from −40 to 120°C, which is 64.5ppm/$^0$C. The output voltage increases with the temperature beyond 94°C because PTAT contribution is getting dominated compared with CTAT ($V_{th}$ of MOSFETs) contribution due to the opamp offset at high temperature, the opamp offset has increased by almost 400uV. A significant contribution to the ppm sensitivity is because of the opamp offset variation with the temperature (Chahardori et al., 2011). Figure 5 depicts the line regulation, which shows how well the output is regulated against the $V_{dd}$ variation. The nominal output value is 261 mV, and it is very evident that the circuit will work with a minimum supply of 475 mV. In the same Figure, the zoomed-in version has also been shown for the sake of regulation calculation. The output voltage has been dropped by 2.04 mV while reducing the supply from 1 to 0.475 V. Hence the line sensitivity is 3.82 mV/V.

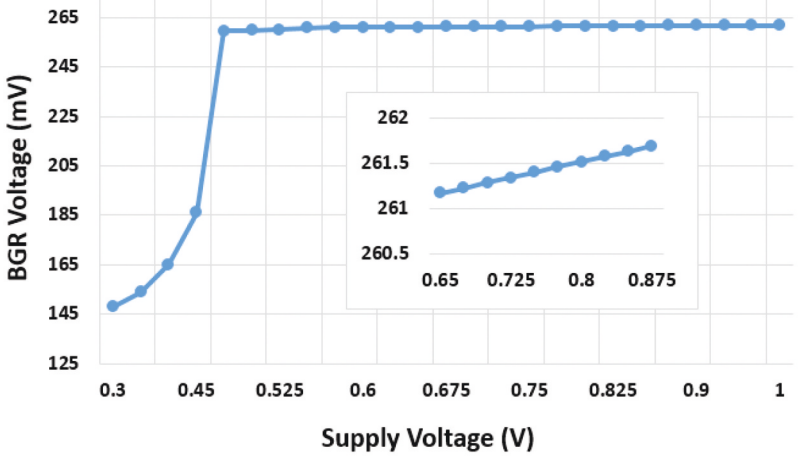


Figure 5. Line regulation at room temperature and typical process corner.

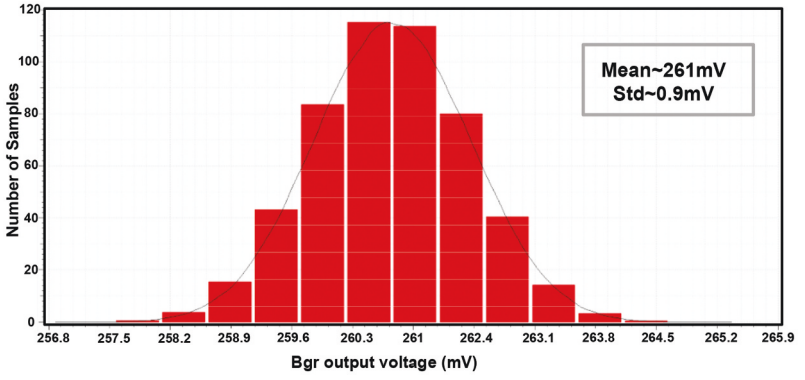


Figure 6. Histogram of the output voltage.

Figure 6 shows the mismatch effect on the reference voltage. It shows the 200 samples Monte-Carlo simulation. The mean of the simulated distribution is 261 mV and a standard deviation of 0.9 mV (0.344% accuracy). Hence 99.97% of the fabricated chips will result in an output voltage in the range of 258.3–263.7 mV. Due to the heavy integration of Digital Signal Processing (DSP) in present-day chips, supply noise is one of the most significant problematic noise sources for sensitive circuits like the BGR, so the power supply effect on the output voltage needs to be studied for the entire frequency range of interest (Marella & Sapatnekar, 2013). Figure 7 shows the simulated Power Supply Rejection Ratio (PSRR) results in −60 dB isolation at low frequency and −15 dB at 300 KHz. Figure 8 shows the simulated noise spectral density, which shows the −142 dB at low frequency and −185 dB at 10 MHz. Up to 100 KHz, most of the noise has been dominated by the flicker noise, and integrated noise over the simulated frequency range is 1.2 μV.

Table 1 shows a summary comparing the performances of the proposed work presented here with current solutions. It shows that the proposed work requires a lower supply voltage (475 mV) compared with the listed state-of-the-art solutions in Table 1. Furthermore, this proposal occupies much less silicon area as it does not require any BJT devices or large PMOS devices. Compared to (Perry et al., 2007), The proposed work

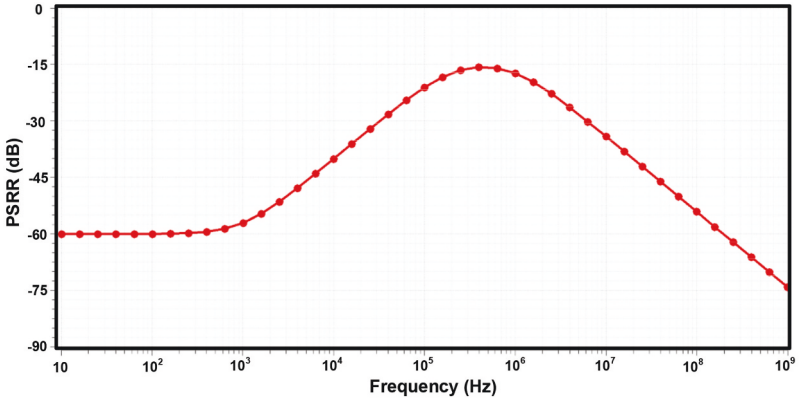


Figure 7. Simulated PSRR at room temperature and 0.8 V power supply voltage.

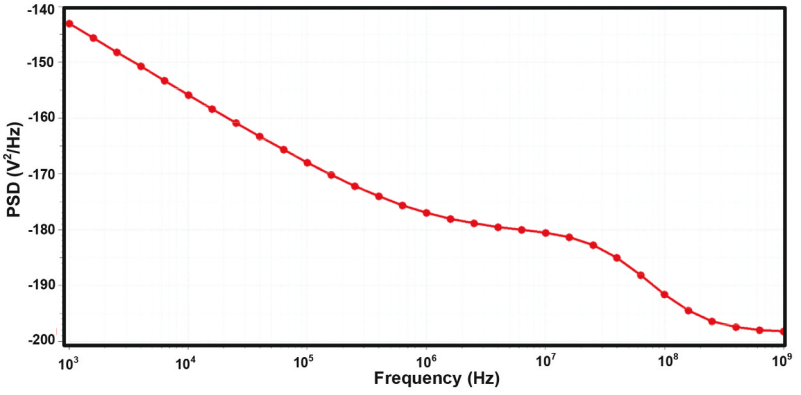


Figure 8. Input referred spectral density.

Table 1. Performance comparision.

| Parameter | Navarro & Ishibe, (2011) | Perry et al., (2007) | Shetler et al., (2015) | Proposed work |
|---|---|---|---|---|
| Supply Voltage (V) | 0.8 | 1.4 | 1.8 | 0.475 |
| Noise (μV) | NA | 9.1 | NA | 1.2 |
| Current consumption (μA) | 6.17 | 115 | NA | 11.2 |
| Temp coeficient (ppm/$^0$C) | 21 | 12.4 | 23.2 | 64 |
| PSRR (dB) | −70 | −68 | NA | −80 |
| Area (mm$^2$) | 0.042 | 1.2 | NA | 0.02888 |

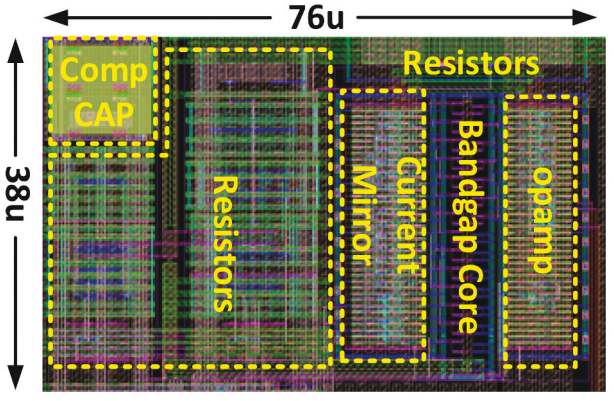


Figure 9. The layout of the total implementation.

presented in this paper consumes ten times less power. Figure 9 shows the layout of the proposed amplifier. Every transistor has been laid with the mismatch and latch-up as the primary concern. All NMOS devices were kept in a deep n-well to protect them from the substrate noise. Enough dummy devices have been kept on both sides of the critical devices to mitigate STI and n-well effects (Nagulapalli et al., 2020, 2021).

## 5. Conclusion

A CMOS based bandgap voltage reference was proposed in this paper, which is powered from a 475 mV power supply. Hence it is very suitable for low power applications. This is the first reported BJT less design with the ultra-low voltage supply. Additionally, the proposed work occupied the smallest silicon area with better PSRR at low frequency (−80 dB). The power consumption of the proposed work, at 5.32μW, is less compared with the listed state-of-the-art solutions in Table 1 while exhibiting outstanding 1.2 μV RMS noise.

## Disclosure statement

No potential conflict of interest was reported by the author(s).

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