CMRR-Bandwidth Extension Technique for CMOS Differential Amplifiers

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Abstract

An exemplary design demonstrates how to extend the common-mode rejection ratio (CMRR) bandwidth of a CMOS differential amplifier. The design presented uses MOSFETs with a channel length of 180nm. A novel circuit technique is employed that partially compensates for the output capacitance of the tail current sink, thereby more than quadrupling the CMRR bandwidth in the example considered.

Keywords: (MOSFET differential amplifier, Common-mode-rejection-ratio, Bandwidth)

1. Introduction

The primary function of a differential amplifier is to produce an output signal that is a linearly amplified version of the normally small difference between two input signals, while rejecting the larger part of the two input signals that are common to both of them. The extent to which it is able to do this successfully is quantified by the 'Common-Mode-Rejection-Ratio' (CMRR), an important parameter in differential amplifiers for many applications, particularly in medical instrumentation [1]. The most commonly encountered common-mode voltage is line or mains interference, at 50Hz or 60Hz. However, with increasing use of switched-mode power supplies and other higher frequency generators, good CMRR at higher frequencies is becoming more important to reduce the amplitude of high frequency common-mode signals in precision instrumentation applications. There have been many improvements to the classical differential pair amplifier [2-4] that improve the CMRR. However, almost all increasing the low frequency CMRR by reducing the common-mode gain, but little has been published to date to address the need for higher CMRR bandwidth performance. This paper outlines a circuit technique that specifically addresses this issue by reducing the tail sink-current capacitance significantly, resulting in a substantial increase in the CMRR bandwidth. Simulation results for an exemplary MOSFET source- coupled differential design, illustrate the advantage of the technique. It produces a four-fold CMRR bandwidth improvement.

2. Normal Circuit Operation

The amplifier shown in Fig.1 is a standard type of MOSFET directly-coupled differential amplifier, appropriately labelled for the discussion that follows. It is well-known that such a source-coupled differential pair amplifier provides good performance provided M_1 and M_2 are well-matched. That is achievable with good IC design techniques, such as the use of common-centroid layout methodology.

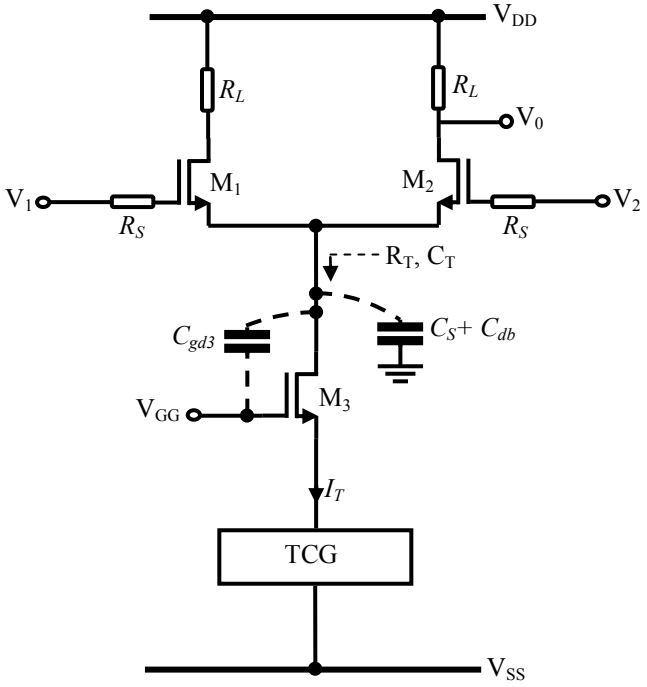

Fig. 1. Typical CMOS differential amplifier circuit
R_T, C_T, C_{dg3}, C_S and C_{db} are defined in the text

M_3 is in the common-gate connection with its gate connected to *DC* voltage V_{GG} , where $V_{DD}>V_{GG}>V_{SS}$. The drain current I_T is supplied by the Tail Current Generator (TCG) connected to its source. TCG can be merely a resistor but is often a current generator in order to increase the incremental output resistance, R_T, seen looking into the drain of M_3. This needs to be a high value for a low common-mode gain and hence a high CMRR at low frequencies. TCG will have an unavoidable nodal capacitance, C_T, associated with it. This needs to be low to maximize the CMRR bandwidth.

The amplifier inputs v_1 and v_2 and, in this particular case, the single output v_0 can each be considered to comprise two components, (i) a differential-mode component,v_d, and (ii) a common-mode component, v_c.
Thus,

$$v_1 = v_c + \tfrac{1}{2}v_d \tag{1}$$

$$v_2 = v_c - \tfrac{1}{2}v_d \tag{2}$$

and,

$$v_0 = A_d v_d + A_c v_c \tag{3}$$

The differential-mode voltage gain, A_d , and the common-mode voltage gain, A_c , are defined as follows,

$$A_d = \left.\frac{v_o}{v_d}\right| \text{With } v_c = 0 \tag{4}$$

and,

$$A_c = \left.\frac{v_o}{v_c}\right| \text{With } v_d = 0 \tag{5}$$

The CMRR, denoted here by the symbol ϱ, is defined as,

$$CMRR = \varrho = \left|\frac{A_d}{A_c}\right| \tag{6}$$

A_d, and A_c are frequency-dependent, hence so too is ϱ. For the determination of A_d the differential-drive considered, the long-tailed pair, formed by M_1, M_2 and its common-source tail current I_T, is imagined to be reconfigured as two common-source half circuits. By inspection, A_d has a *DC* and very-low-frequency gain of magnitude $g_m.R'_L/2$, where g_m is the transconductance of each of M_1, M_2 at a *DC* operating current $I_T/2$ and $R'_L = R_L // r_{ds}$ (r_{ds} being the drain-source incremental resistance of each of the MOSFETs). Based on the work of [5], with appropriately modified notation, A_d exhibits a dominant pole at a radian frequency ω_{pc}.

$$\omega_{pd} = \frac{1}{R_S C_{gs} + R_S C_{gd}(1 + g_m R'_L) + R'_L (C_L + C_{gd})} \tag{7}$$

In this equation, C_{gs} and C_{gd} have their usual MOSFET significance and C_L is the load capacitance existing at the drain of each of M_1, and of M_2.

For the determination of A_C, the circuit is regarded as two separate stages, each having a source load $2Z_T$ (where, $Z_T = R_T // C_T$ and the drain load $Z_L = R'_L // C_L$)
Hence, in terms of the complex frequency variable *s*,

$$A_c(s) = -\frac{Z_L}{2Z_T} = -\frac{R'_L}{2R_T} = \frac{(1 + sR_T C_T)}{(1 + sR'_L C_L)} \tag{8}$$

Thus, A_c exhibits a *DC* and very low-frequency gain of magnitude $-R'_L/2R_T$, and a pole at a radian frequency ω_{pc} and zero at ω_{zc},

$$\omega_{pc} = \frac{1}{R'_L C_L} \tag{9a}$$

$$\omega_{zc} = \frac{1}{R_T C_T} \tag{9b}$$

C_T comprises three capacitances, C_{gd3} and C_{db3}, respectively the drain-gate and drain-substrate capacitance of M_3, together with C_S the stray capacitance at its drain, thus,

$$C_T = C_S + C_{db3} + C_{gb3} \tag{10}$$

The zero at ω_{zc} on the plot of *Ac* versus ω now appears as a pole on the CMRR-frequency plot in addition to the pole at ω_{pc}, and the pole of ω_{pc} on the *Ac* plot appears as a zero on the CMRR plot. The nature of existing circuit designs is such that $\omega_{pc} >> \omega_{zc}$, because $R_T >> R'_L$, R_S. Furthermore, $\omega_{pc} >> \omega_{zc}$ because, even if $(C_T + C_{gd2}) = 10C_T$, $R_T >> R'_L$, R_S *(e.g,.* $R_T >> 100\ R'_L$*).*

Consequently, ω_{zc} is the dominant pole on the CMRR-frequency plot, and effectively determines the CMRR -3dB bandwidth because of the relationship of ω_{zc} to ω_{pd} and ω_{pc}. Thus, on a Bode plot of ϱ versus ω , ϱ is constant at a value $\varrho_o = g_m.R_T$ only up to a frequency ω_{zc}. From the above discussion,

$$\varrho_o \omega_{zc} = g_m / C_T \tag{11}$$

So, for a specified and practically achievable ϱ_o, ω_{zc} is maximized by minimizing C_T. This can be done, as described below, by using a MOSFET variant of an elegant bipolar technique outlined by Baxandall and Swallow [6], but seemingly neglected in the literature until investigated in detail in recent years by Terzopoulos [7].

In passing, it is worth noting that the constancy of the product $\varrho_o \omega_{zc}$ with variation in R_T is analogous to the constancy of the gain-bandwidth product in resistively loaded common-source (and common-emitter) voltage amplifier stages.

3. Improved CMRR Circuit

The circuit shown in Fig.2 is a modified version of Fig.1, in that an additional common-gate connected P-MOS transistor, M_4, is now incorporated into the circuit to compensate for C_{dg3}, and M_4 operates with its gate connected to a *DC* supply, V_{XX}, where, $V_{DD} > V_{XX} > V_{SS}$, and its source is connected to the gate of M_3. It is supplied with a *DC* bias current, I_X, and its drain is connected to the source of M_3. A change in the drain voltage of M_3 gives rise to a change i_j in the gate-drain capacitance, C_{dg3}.

A part, i_k , of i_j is returned to the source circuit of M_3. Hence, at the drain terminal of M_3, C_{gd3} appears to be a substantially smaller capacitance C'_{gd3}.

$$C'_{gd3} \approx C_{gd3}\left|1-\frac{i_k}{i_j}\right| \qquad (12)$$

The nodal capacitance at the drain of M_3, which was designated C_T in Fig.1, now becomes C'_T

$$C'_T = C_S + C_{db3} + C_{gb3}\left|1-\frac{i_k}{i_j}\right| \qquad (13)$$

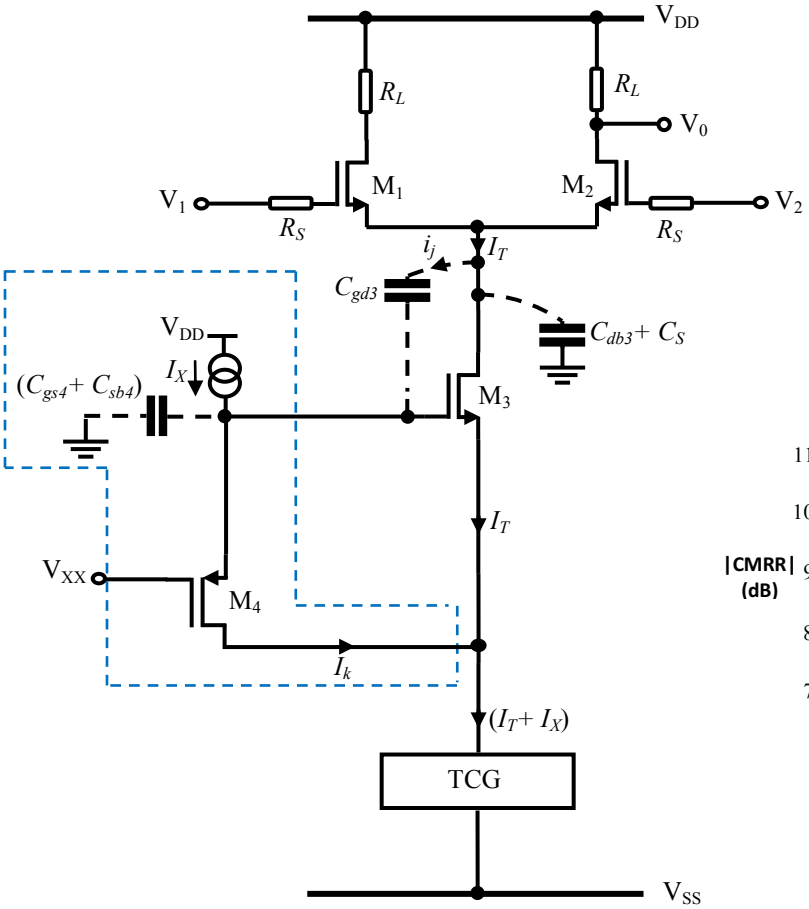

Fig. 2. Proposed differential amplifier configuration.
It is a modified vesion of Fig.1. M_4, with its bias components, shown inside the coloured contour line, is intended to compensate for the existence of C_{dg3}

If ω'_{zc} is the new CMRR bandwidth then,

$$\omega'_{zc} = (1 / C'_T\ R_T) > \omega_{zc} \qquad (14)$$

The condition $\left|\frac{i_k}{i_j}\right| = 1$ is not possible because of current lost in the gate-source capacitance, C_{gs4}, and source-substrate capacitance, C_{sb4}, of M_4.

However, the ratio $\left|\frac{i_k}{i_j}\right|$ can be made to approach unity by suitably proportioning the gate width of M_4 relative to that of M_3, and by choice of the ratio $\left[\frac{I_X}{I_T}\right]$, for a given value of I_T.

4. Results and Discussion

To demonstrate the proposed bandwidth extension technique, Fig.2 was simulated for an illustrative, but not necessarily optimised, design using CADENCE/ VIRTUOSO, with process tsmc18rf technology. The channel length for all the transistors was 180nm, and the gate widths of corresponding transistor number subscript, were: w_1=w_2=1µm; w_3= 10µm; w_4=20µm. Test conditions were; R_S=0, V_{DD}=5V; V_{XX}=-2.5V; V_{SS}=-5V; V_{GG}=1V; I_X =0. 1mA; I_T =1mA. I_X was the output of a PMOS 1:1 current mirror with a cascode output stage. TCG was an NMOS 1:1 current mirror with a double-cascode output stage added to give increased incremental output resistance.

In the test mode, Fig.2 was used throughout. In the first series of tests the CMRR-frequency performance of Fig.1 was simulated. To achieve this the drain terminal of M_4 was disconnected from the source of M_1, and connected instead to V_{SS}.
The output of the TCG was set to 1mA. Graph (A) in Fig.3 shows the resulting CMRR performance.

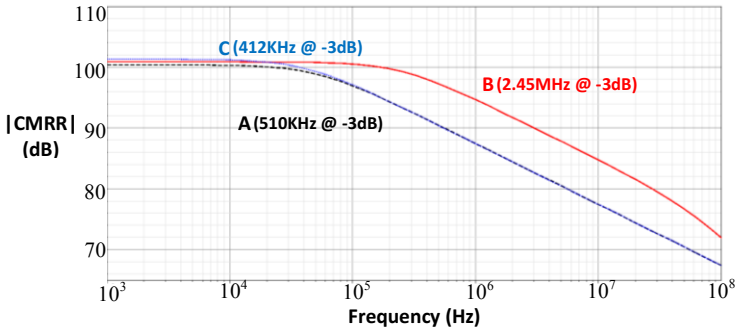

Fig. 3. CMRR~Frequency dependence
Curve A refers to the circuit of Fig. 1. and B to the circuit of Fig. 2.
Curve C refers to the circuit of Fig. 1. with increased I_T

In a second series of tests, intended to show the improvement in CMRR bandwidth, the circuit shown in Fig.2 was used with the output of the TCG set to 1.1mA. Thus, M_3 operated under the same *DC* conditions for both tests. The CMRR performance is shown by Graph (B) in Fig.3. The CMRR

bandwidth, ω_{zc} as determined from the phase-shift corresponding to the -3dB points, is more than quadrupled.

In a third series of tests to see what happens when the design of Fig.1 was operated with same total current as the proposed design of Fig.2. I_T in Fig.1 was 1.1mA, the current used for Fig.2. The resulting CMRR-frequency plot is curve C, which shows a lower cut-off frequency than curves A and B. Curves A, B and C all have slightly different values of ϱ_o . This is because the different *DC* bias currents in the tests leads to differing values of the small signal parameters g_m and r_{ds} of the MOSFETs (and hence differing values for R_T). Curves A and C are for the same C_T , but the effective R_T of C_T is greater than that of A. In accordance with the discussion in section 2, above, this means a lower ω_{zc} but that the curves are coincident well above their cut-off frequencies.

It should be noted that the load resistors (R_L) have been used to simplify the discussion and analysis. The resistive loads gave a low frequency value of A_d in the region of 60dB. In practice it is most likely that P-MOS transistors configured as active load current sources would be used instead to provide a considerably higher A_d . However, the method of increasing bandwidth of CMRR which has been presented here is still maintained with active loads in the drains of M_1 and M_2.

In this paper a MOSFET differential amplifier has been considered because of the growing importance of CMOS in analogue circuit design. However, depending on the application, bipolar transistors maybe employed, instead of MOSFETs, with M_1, M_2, M_3, M_4 being replaced by bipolar transistors Q_1 , Q_2, Q_3, Q_4 respectively. Then the presence of Q_4 not only partially compensates of the collector-base capacitance of Q_3 but, as shown in [7], it also increases the incremental output resistance seen looking into its collector.

5. Conclusions

The addition of only one transistor, plus associated bias circuitry, into a conventional source-coupled differential amplifier has been shown to extend the CMRR bandwidth substantially. This performance improvement is a result of local feedback reducing the source-coupled nodal capacitance of the differential pair. This technique is primarily applicable to an integrated circuit realization of the source-coupled differential amplifier because closely matched transistors operating at the same temperature are essential for satisfactory operation.

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