A Single BJT 10.2 ppm/^{0}C Bandgap Reference in 45nm CMOS Technology

R. Nagulapalli, K. Hayatleh, S. Barker
Oxford Brookes University, Wheatley Campus, Oxford
OX33 1HX United Kingdom.

***Abstract*—Bandgap reference using 2 BJT devices are well explored in the literature. Usually, less number of BJT's would reduce the cost of the chip in modern CMOS technologies. A single BJT based reference was discussed here. V_{BE} of the BJT has been used as CTAT voltage and a CMOS differential pair offset voltage based PTAT generation circuit used to generate zero temp coefficient reference. A prototype was developed in 45nm TSMC CMOS technology and post-layout simulations were performed. Designed for a nominal voltage of 525mV with 10.2ppm/^{0}C temperature coefficient. Its supply sensitivity is 0.4% and works with 1V power supply. The proposed solution consumes 51.8µW power from 1V power supply and occupies 2478 µm^{2}silicon area.**

Keywords—Bandgap, PTAT, CTAT, PVT variation, Noise, Stability.

I. INTRODUCTION

The Bandgap reference (BGR) is a key circuit in low power applications like bio-medical, internet of things (IOT) and passive RFID devices, where they must operate with extremely low power for long time battery [1]. The resolution of the bio-medical transceiver depends on the o/p of the ADC accuracy, which depends on the ppm accuracy performance of the BGR. Also, there is an interest in building the circuit in the modern CMOS cutting technology due to the scaling nature and low power DSP capabilities. But unfortunately CMOS technology poses few design changes to the analog IC design. Mainly the supply voltage has been decreased to around 1V, which decreases the voltage headroom available and cascade opamps realization almost impossible. Also the flicker noise performance of the transistors has degraded by more than a decade at a given frequency and flicker noise corner frequency has increased by almost 3 times. All the above-mentioned challenges make ultra-low power circuit realization is so difficult [2].

There has been a lot of research carried out to improve the bandgap accuracy, power consumption and minimum silicon area. [3] proposed first generation BGR which results in 1.23V o/p. This topology requires 3 BJT's, which is not very compatible with CMOS technology. Also the BGR voltage needs to be much less than 1.23V because the supply voltage is getting down hence there is a need for sub-bandgap circuits. Fig:1 shows the successful low voltage bandgap, which uses only 2 BJT's.

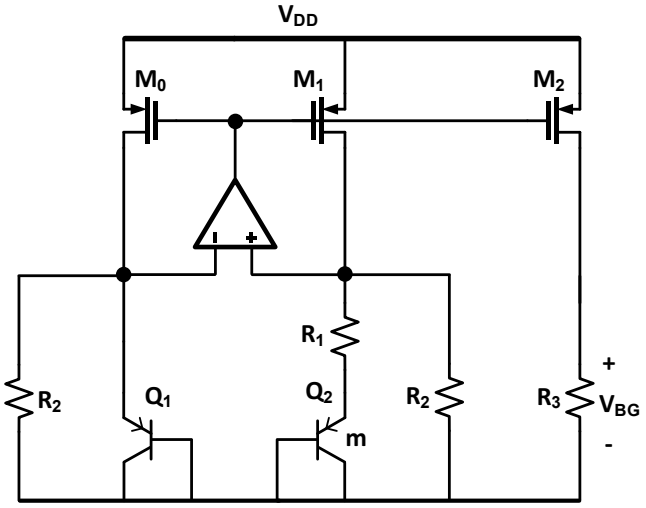

Fig. 1. Traditional current mode sub-bandgap reference.

The principle behind any BGR circuit is to generate a Complimentary To Absolute Temperature (CTAT) and Proportional to Absolute Temperature (PTAT) voltages and adding them in the scaled proportion to get cancel both temp coefficients. The VBE of the forward bias BJT will decrease with the temperature with 2mV/^{0}C temp coefficient. The current flowing through the resistor R2 will have CTA nature.

$$I_{CTAT} = \frac{V_{BE}}{R_2}$$

A typical choice for the PTAT generation is the V_{BE} difference between the two forward bias voltages whose current density is different. In the above fig:1, the voltage across R_1 is the having PTAT nature and as expressed as below.

$$I_{PTAT} = \frac{V_T \ln m}{R_1}$$

The output voltage can be expressed as follows.

$$V_{BG} = \frac{R_3}{R_2}\left(V_{BE} + \frac{R_2}{R_1} V_T \ln m\right) \qquad (1)$$

From (1), it is clear that the o/p voltage can be scaled with R_3,R_2 and temperature coefficient can be adjusted with R_2,R_1. This is an excellent improvement in this circuit compared to other proposals. But this BGR has also several disadvantages [4]. Mainly the BJT's are shunted by R_2, which will make the three undesirable operating points

compared to 2 points in the traditional BGR, which increases the chances of failure in real-time. The resistor R_2 is typically in the range of 500K, which will have a significant impact on the area. Also this uses two BJT devices, this is will add significant cost to the fabrication. In this paper we are proposing a technique that will have similar advantages of the current mode bandgap with single BJT and no multiple undesirable operating points.

The rest of the paper has been organized as follows. Section II analyses PTAT generation technique with the help of the differential pair. section III explains proposed bandgap reference technique and finally section IV summarizes the post-layout simulation results.

II. PTAT VOLTAGE GENERATION

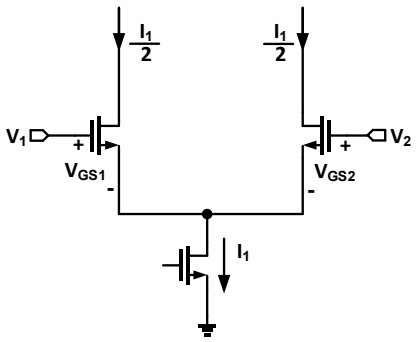

Fig. 2. PTAT voltage generation

Fig. 2 shows the conventional differential amplifiers without having any load devices. Assume it has been biased with two bias voltages from the self-bias circuit (means V_1,V_2 will be derived from a bias circuit). This structure can be exploited to generate PTAT voltage by biasing the devices. When the V_{DS} of the transistor >4KT/q, the V_{GS} can be expressed as follows.

$$V_{GS} = V_{th} + \eta V_T \ln\left(\frac{I_d}{\frac{W}{L} I_0}\right) \qquad (1)$$

Where η is the subthreshold slope factor, V_T is the thermal energy and I_0 is the sub-threshold current. The voltage difference between the two gates can be expressed as follows.

$$V_{GS1} - V_{GS2} = \eta V_T \ln\left[\left(\frac{W}{L}\right)_1 / \left(\frac{W}{L}\right)_2\right] \qquad (2)$$

This reveles that that V_{gs1} linearly increases with the temperature, hence it can be used as PTAT voltage. Also, it depends only on the ratio of the aspect ratio of W_1,W_2 transistors, hence it is independent of PVT (Process,Voltage,Temperature) variations [5]. This result is very similar to BJT based PTAT generation and the proposal doesn't require process expensive BJT's. In general, BJT based PTAT will have several errors related to the current gain (beta). The above circuit is exactly similar to a traditional differential pair except for the fact that it needs a method to inject a systematic offset. Hence we need to find a way to close the negative feedback loop around the structure to avoid the current steering to one side of the differential pair. Fig:3 shows the simulated PTAT voltage across temperature in TT corner.

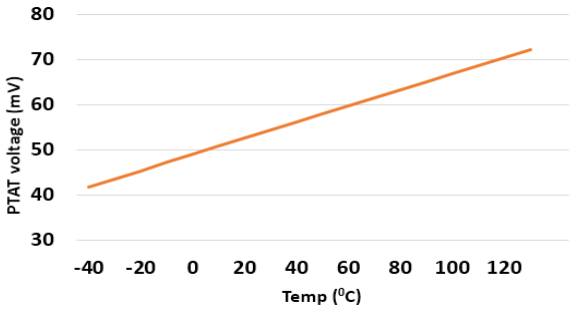

Fig. 3. PTAT voltage generation

III. PROPOSED TECHNIQUE

To arrive at the final circuit, the following thought process can be used. Eventually one needs to find a way to generate PTAT, CTAT circuits, and a scaled summing network to realize a bandgap reference [6]. As explained in the previous section, PTAT was generated using differential pair offset voltage. A BJT Base to Emitter voltage (V_{BE}) can be used as a potential candidate for the CTAT generation. As the last step a scaled summation network required. The PTAT voltage across the differential pair input would be difficult to add to the CTAT. For that, creating PTAT nature current and generating again PTAT voltage in series with a scaled version PTAT would be easy to realize with lesser power consumption. Fig:4 shows the proposed circuit. M_1, M_2, M_3, M_4 and M_5 form the differential pair for the PTAT voltage generation and the voltage difference between the nodes x,y is PTAT. A potential divider R_1,R_2 with a biasing transistor M_7 forms the PTAT current branch, since the current will be decided by the resistor R_1. BJT (Q_3) and biasing transistor M_8 forms the CTAT voltage generation branch and node Z will have CTAT nature [7].

$$V_{BG} = V_{BE}\frac{R_2}{R_1+R_2} + \frac{V_{PTAT}}{R_1}\frac{R_2R_3}{R_2+R_3}$$

$$= V_{BE}\frac{R_2}{R_1+R_2} + \frac{\eta V_T \ln\beta}{R_1}\frac{R_2R_3}{R_2+R_3} \qquad (3)$$

Where β is the ratio of M_1 to M_2 aspect ratio. From the simulation, the temperature coefficient of CTAT (V_{BE}) is -1.6mV/^{0}C and PTAT is 0.087mV/^{0}C. To find the relation for getting a minimum temp coefficient for the o/p voltage, it's derivative wrt to temperature should be zero.

$$\frac{\partial V_{BG}}{\partial T} = \frac{\partial V_{BG}}{\partial T}\frac{R_2}{R_3+R_2} + \frac{\partial V_T}{\partial T}\frac{\eta \ln\beta}{R_1}\frac{R_2R_3}{R_2+R_3} = 0 \qquad (4)$$

Let's assume R_3=2R_2 for simplicity and (4) can be simplified as follows.

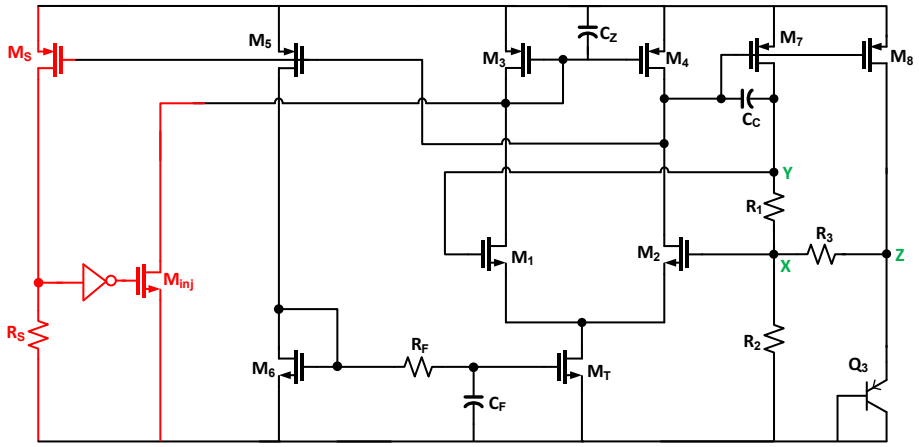

Fig. 4. Effect of g_{m7} on the frequency response

Let's assume $\beta = 8$ for the matching comfort in the layout.

$$\frac{\partial V_{BG}}{\partial T} = \frac{\partial V_{BG}}{\partial T}\frac{1}{3} + \frac{\partial V_T}{\partial T}\frac{2\ln\beta}{3}\frac{R_2}{R_1} = 0 \qquad (5)$$

By substituting these relations into (5), the desired R_2/R_1 can be calculated as 4.59 for the minimal temp coefficient of the o/p voltage. The advantages of the prosed circuit over the existing state of the art is, it only requires single BJT and less number bias current branches, hence very low power suitable for the IOT and bio-medical applications [8]. The value of the bandgap voltage is approximately 520mV. The proposal has several advantages compared to existing designs[14]. The sub-bandgap voltage can get as low as possible, by choosing the R_2,R_3 ratio without effecting the temp co. Also like any bandgap, this also requires a startup circuit. M_S, M_{INJ},R_S forms the startup circuit, when the current is zero the M_{INJ} pulls kick-up current from the reference and enables the reliable operation[10].

IV. Simulation Results.

The proposed technique has been implemented in 65nm CMOS technology and the ratio of resistors was calculated according to the equation (5). Fig. 5 shows the temperature sensitivity of the bandgap reference while temperature swept from -25 to 125^0C. This has been simulated for several MOS process corners (TT, SS, FF, SF). The worst-case temp sensitivity is 1.9mV, which is 10.2ppm/^{0}C. The closed-loop stability simulation of the proposed circuit is 67dB low-frequency gain with 55^0 phase margin. This is good enough for an acceptable transient response. The miller frequency compensation has been used around M_7 transistor, in-order to save silicon area. Fig:6 shows the noise of the proposed circuit, which is -160dB at 1KHz and -200dB at 100MHz. The integrated rms noise within the frequency band of interest is 2.3uV, which 6 times better than [11]. Every bandgap has to exhibit the less dependent on the power supply, which is quantified as the line-sensitivity. SOC based implementations use an explicit Low Voltage Dropout Regulators (LDO) to get better than -30dB PSRR which will be very beneficial but at the cost of significant power and silicon area (decap)[15]. Fig:7 shows the line sensitivity, which shows 0.4% sensitivity to the supply. Up to 0.95V supply voltage circuit is working fine, but less than that transistors are entering into the linear region and o/p voltage affecting very badly. Fig.8 shows the Layout of the proposed design which occupies 42*59um^2 active silicon area. The common-centroid layout technique has been used to improve the matching of the differential pair devices and the interdigitating technique used for current mirrors to minimize the mismatch induced current error [9]. Special care has been taken to minimize the STI and Well proximity effects such as adding dummy active on both sides of the devices and maintaining enough separation between the PMOS devices and nwell boundary [12].

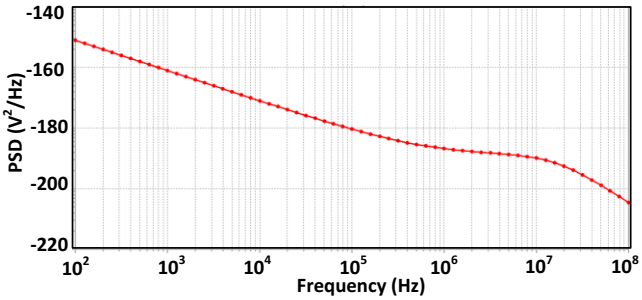

Fig. 5. Noise frequency response.

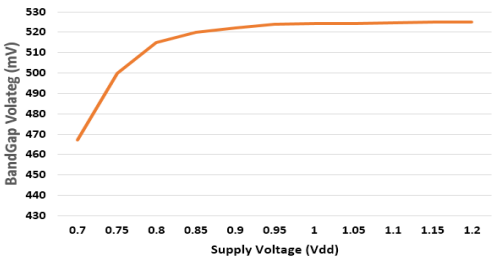

Fig. 6. Line sensitivity

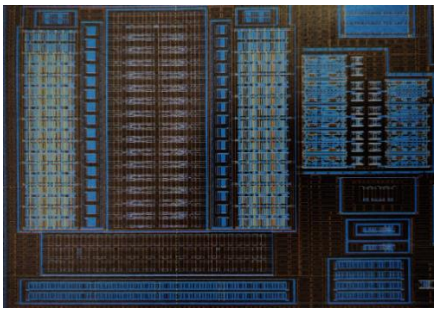

Fig. 7. Layout of the Proposed technique

V. Conclusion

In this paper a novel single BJT based bandgap reference circuit has been proposed. BJT voltage has been exploited for the ctat voltage generation and a differential pair based ptat circuit has been proposed. It exhibits 10.2ppm over the temperature range of interest. As future work, improving PSRR will be considered as it is very important in the present days' applications. Also considering nano-watt power level would make solution suitable for the wireless applications.

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