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Theoretical Study of the Circuit Architecture of the Basic CFOA and Testing Techniques

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Abstract

This paper examines the closed-loop characteristics of the basic CFOA, and in particular, the dynamic response. Additionally, it also examines the design and advantages of the CFOA regarding its ability to provide a significantly constant closed-loop bandwidth for closed-loop voltage gain. Secondly, the almost limitless slew–rate provided by the class AB input stage that makes it superior to the VOA counterpart. Additionally; this paper also concerns the definitions and measurements of the terminal parameters of the CFOA, regarded as a 'black box'. It does not deal with the way that these parameters are related to the properties of the active passive and active components of a particular circuit configuration. Simulation is used in terminal parameter determination: this brings with it the facility of using test conditions that would not normally prevail in a laboratory test on silicon implementations of the CFOAs. Thus, we can apply 1mA and 1mV test signals from, respectively, infinite and zero source impedances that range in frequency from d.c to some tens of GHz. Also, we assume the existence of resistors with identical Ohmic value and very high value ideal capacitors. Where appropriate, practical test methods are referred to physical laboratory prototypes.

Keywords: (VOA; CFOA; CMRR; Bandwidth; Input referred offset voltage; Slew-rate)

1. Introduction

The development of very large scale integration (VLSI) technology, together with the ever increasing demand for fully integrated systems containing a larger number of both analog and digital circuits on a single chip, has ensured continued interest in analog circuit design. In fact, analog circuits such as continuous-time filters, sinusoidal oscillators, analog to digital (A/D) and digital to analog (A/D) converters, voltage comparators, current and voltage amplifiers, rectifiers, etc. are unavoidably analog circuits, and cannot be realized by digital techniques. Moreover, new applications continually appear which require the design of new analog topologies to ensure the trade-off between the need for speed and low power [1], [2], [3], [4] and [5]. Historically, the operational amplifier has formed the fundamental building block in analogue integrated circuit design. More recently, new integrated analogue circuit applications have emerged, along with their new performance requirements. In analogue circuit design, there is also often a significant demand for circuits with a performance suited to digital signal processing applications [6] and [7]. Analogue circuit design has historically been viewed as a voltage dominated form of signal processing. Only recently, current-mode analog circuits have been used to implement analog functionality. In current- mode circuit description, the input and the output are both taken in the current form rather than in voltage form. A current- mode signal processor can be defined as a circuit in which certain critical parts or all of the circuit use current as the preferential active variable, rather than voltage [8] and [9]. At high gains, the constant gain-bandwidth product of voltage-mode operational amplifier (VOA) circuits limits the

bandwidth [10]. Moreover, the large-signal, high frequency is affected by limited slew-rate of the operational amplifier [11]. Thus for wide bandwidth, low noise, low distortion and fast slew rate applications VOA is not recommended [12] and [13].

The current-mode approach [14], and [15] which considers the information carried by time-varying currents, provides a new viewpoint on integrated circuit operation, even if it only means examining older circuits with a view towards designing differing solutions to their problems. Current-mode circuits provide some significant advantages: Firstly, high performance amplifiers are not required as the circuits do not provide a high voltage gain. Secondly, they can be designed almost entirely with transistors, thus eliminating the need for close tolerance passive components. Therefore, current mode circuits are highly compatible with typical digital applications. Additionally, they demonstrate considerable speed, bandwidth and accuracy performances [16]. The application of filters and oscillators in communication circuits needs extended high frequency performance in fully integrated circuit form [17], [18], [19] and [20]. Circuit designers began to search for a more suitable active element in order to provide the necessary gain without imposing severe frequency limitations due to the fixed gain-bandwidth product [21] and [22]. At the same time, endeavors were made to keep the circuitry simple so that it can be realized in IC technologies, thereby enabling easy synthesis procedures for active circuits, and hence, there are many active building blocks introduced for this purpose. In addition to the advancement in current-mode analog signal processing, another particular development is the emergence of new current-mode analog building blocks, amongst which the most prominent and popular has been the well-known current-mode circuit, the Current-Feedback Operational Amplifier (CFOA) [23] and [24]. In contrast to the VOA, the CFOA can, under certain conditions, amongst other things, exhibit higher bandwidth and better signal linearity [25]. Most CFOA applications are concerned with video signal processing. This is because of the inherently high differential gain and phase performance, along with two other factors. One, for voltage gains up to 10, the CFOA provides a constant closed–loop bandwidth. Two, the provision of an extremely high slew-rate. All of these characteristics are provided by the asymmetric design of the class–AB input stage, sometimes described as a ‘diamond buffer’ which makes the CFOA an extremely useful amplifier for video and telecommunication systems.

This paper is primarily concerned with the analysis of the closed-loop output resistance and the closed-loop low frequency as well as and D.C. behaviour. In addition to this, the paper is also concerned with the study of the theoretically unlimited slew-rate capability of the CFOA, which provides a low distortion output for large amplitude, high frequency inputs. This paper also critically reviews the techniques for the measurement of key parameters of the CFOA.

2. Closed-loop output resistance

This section considers the closed-loop output resistance R_O of the CFOA, and its relationship to the open-loop output resistance, r_O. Using nodal analysis (to find V_o/I_o) with conductance instead of resistance ($G_G=1/R_G$, etc…)

In Fig.1 CFOA is shown configured as a closed-loop inverting amplifier

For node V_x: $V_x(G_G + g_i) + (V_x - V_o)G_F = 0$

$$\therefore V_x(G_G + g_i + G_F) - V_o G_F = 0 \quad (1)$$

$$\therefore V_x = \frac{V_o G_F}{(G_G + g_i + G_F)} \quad (2)$$

Fig.2 illustrates the small-signal equivalent circuit for the calculation of CFOA closed-loop output resistance.

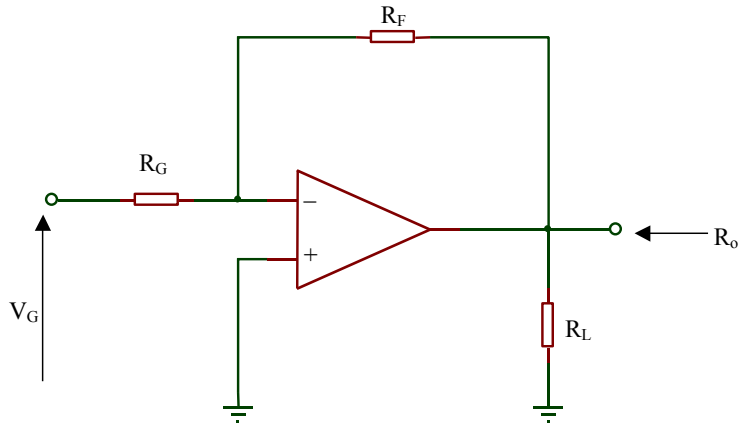

Figure 1: CFOA configured as a closed-loop inverting amplifier to calculate output resistance, R_O

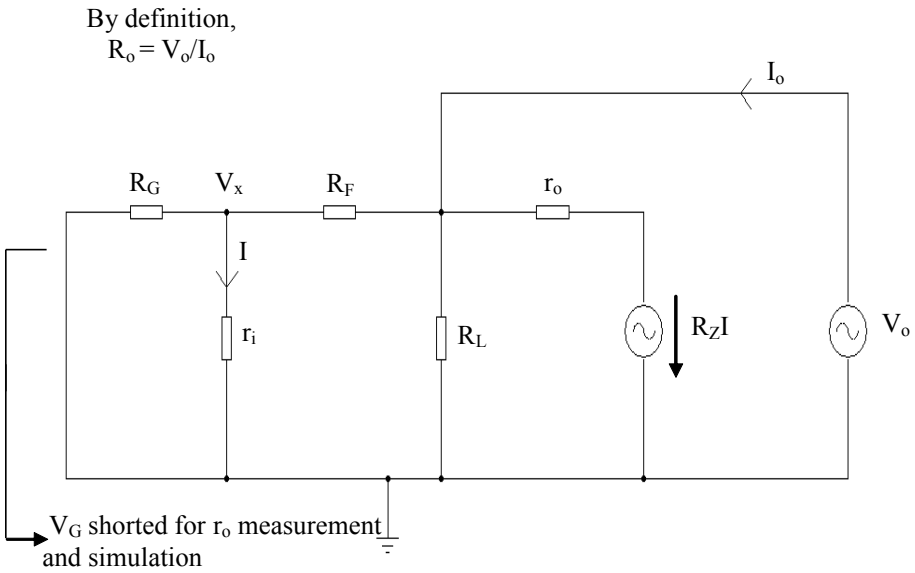

Figure 2: The small-signal equivalent circuit for the calculation of CFOA closed-loop output resistance

As shown below in Fig.3 is a simplified form of Fig.2 using Norton's equivalent.

For node V_o: $(V_o - V_x)G_F + V_o(G_L + g_o) + \frac{V_x R_Z}{r_i r_o} = I_o$

$$\therefore V_x[\frac{R_Z}{r_i r_o} - G_F] + V_o[G_L + G_F + g_o] = I_o \quad (3)$$

Substitute equation (2) into (3), then,

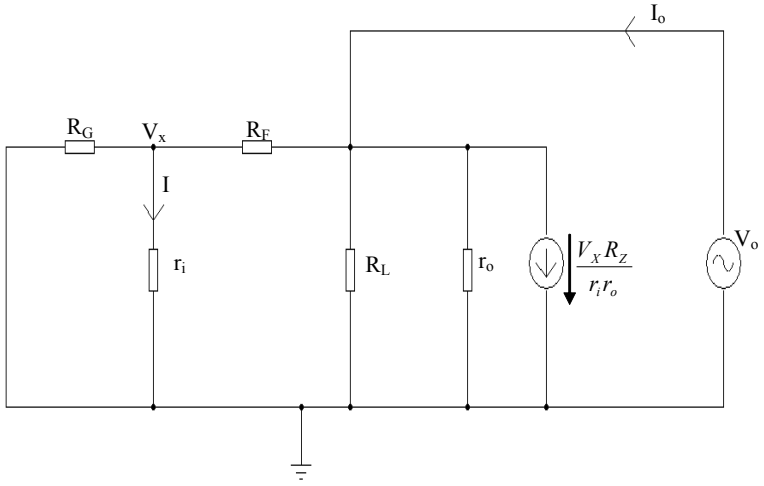

Figure 3: Simplified Norton's equivalent for Fig.2

$$\frac{V_o G_F}{(G_G + g_i + G_F)}[\frac{R_Z}{r_i r_o} - G_F] + V_o[G_L + G_F + g_o] = I_o \quad (4)$$

$$\therefore V_o[\frac{G_F}{(G_G + g_i + G_F)}(\frac{R_Z}{r_i r_o} - G_F) + G_L + G_F + g_o] = I_o$$

(5)

Thus for R_o,

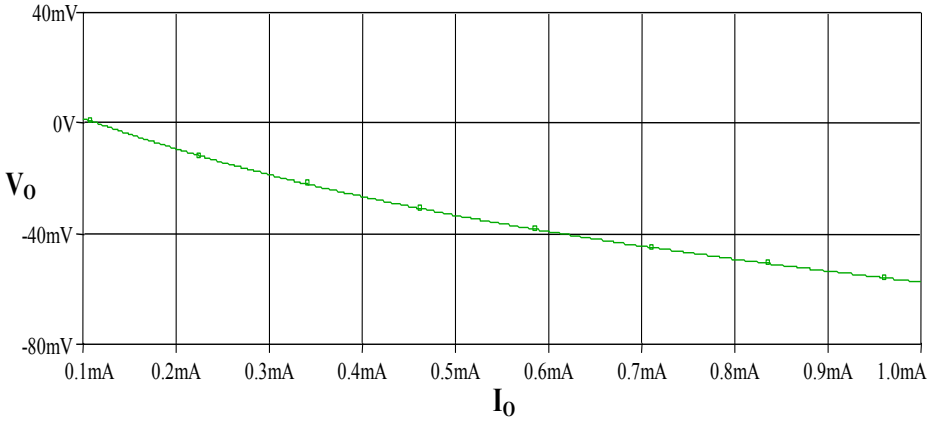

Figure 4: The plot of V_O versus I_O for the basic CFOA on closed loop with I_Q=0.1mA

$$\therefore R_o = \frac{V_o}{I_o} = \frac{1}{[\frac{G_F}{(G_G + g_i + G_F)}(\frac{R_Z}{r_i r_o} - G_F) + G_L + G_F + g_o]} \quad (6)$$

Now rewrite this in terms of resistances instead of conductances to make it easier to follow:

$$R_o = \frac{1}{[\frac{1}{R_F(\frac{1}{R_G} + \frac{1}{r_i} + \frac{1}{R_F})}(\frac{R_Z}{r_i r_o} - \frac{1}{R_F}) + (\frac{1}{R_L} + \frac{1}{R_F} + \frac{1}{r_o})]} \quad (7)$$

Since, in practice, $(\frac{R_Z}{r_i r_o}) >> \frac{1}{R_F}$, and

$$R_o \approx \frac{1}{[\frac{1}{R_F(\frac{1}{R_G} + \frac{1}{r_i} + \frac{1}{R_F})}(\frac{R_Z}{r_i r_o})] + (\frac{1}{R_L} + \frac{1}{R_F} + \frac{1}{r_o})} \quad (8)$$

From previous simulation, $[\frac{1}{R_F(\frac{1}{R_G} + \frac{1}{r_i} + \frac{1}{R_F})}(\frac{R_Z}{r_i r_o})] >> (\frac{1}{R_L} + \frac{1}{R_F} + \frac{1}{r_o})$, Thus

$$\therefore R_o \approx \frac{R_F(\frac{1}{R_G} + \frac{1}{r_i} + \frac{1}{R_F}) r_i r_o}{R_Z}$$

(9)

$$R_o \approx r_o[\frac{R_F(1 + \frac{r_i}{R_G} + \frac{r_i}{R_F})}{R_Z}] \quad (10)$$

This is of the form typical for operational amplifiers,

$$R_o \approx \frac{r_o}{|LG|}$$

where, $|LG|$ is the magnitude of the first-order expression for the low frequency loop gain. Normally $|LG| >> 1$ so $R_O << r_O$. This is borne out by the plot in Fig 4: The slope of Fig 4 at a given I_O gives r_O at that I_O. Note that there is normally a small inductive component in the output impedance because of the presence of emitter-followers at the voltage-follower output. This, of course, does not show up in d.c. measurements.

3. Closed-loop low frequency and d.c. behavior

Fig.5 represents the most general amplifier configuration. Thus:

For V_G=0 it is a non-inverting amplifier, V_S being the input;
for V_S=0 it is an inverting amplifier, V_G being the input;
for $V_S \neq 0$, $V_G \neq 0$ it is a type of differential amplifier;
for V_S=0, $R_G \to \infty$, $V_G \to \infty$, but (V_G /R_G) finite, it is an I/V converter;

At node V_x:

$$(V_x - V_S)g_i + (V_x - V_G)g_G + (V_x - V_O)g_F = 0 \tag{11}$$

$$\therefore V_x[g_i + g_G + g_F] = V_O g_F + V_S g_i + V_G g_G \tag{12}$$

At node V_O:

$$g_F(V_O - V_x) + g_O V_O + R_Z g_i g_O (V_x - V_S) = 0 \tag{13}$$

$$\therefore V_x[R_Z g_i g_O - g_F] = R_Z g_i g_O V_S - V_O[g_O + g_F] \tag{14}$$

But, under normal conditions $R_Z g_i g_o >> g_F$

$$\therefore V_x[R_Z g_i g_O] \approx R_Z g_i g_O V_S - V_O[g_O + g_F] \tag{15}$$

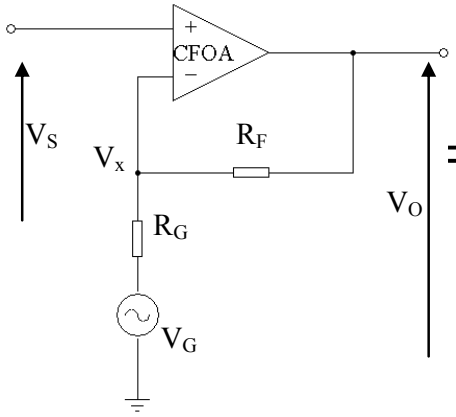

Figure 5: General amplifier configuration

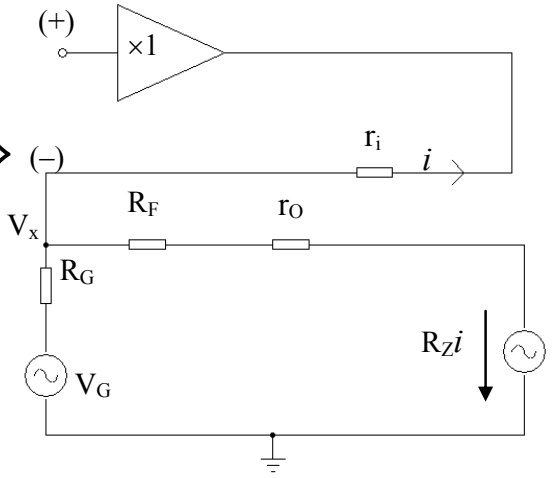

Figure 6: Macro-modelling the circuit of Fig.5

$$\therefore V_x = V_S - \frac{V_O[g_O + g_F]}{R_Z g_i g_O} \tag{16}$$

Substitute for V_x from equation (16) into equation (12).

$$[V_S - \frac{V_O[g_O + g_F]}{R_Z g_i g_O}](g_i + g_G + g_F) = V_O g_F + V_S g_i + V_G g_G \tag{17}$$

$$\therefore -V_O[g_F + \frac{g_O + g_F}{R_Z g_i g_O}(g_i + g_G + g_F)] = -V_S(g_i + g_G + g_F) + V_S g_i + V_G g_G \tag{18}$$

$$\text{or, } V_O[g_F + \frac{g_O + g_F}{R_Z g_i g_O}(g_i + g_G + g_F)] = V_S(g_G + g_F) - V_G g_G \tag{19}$$

$$\therefore V_O = V_S[\frac{(g_G + g_F)}{[g_F + \frac{g_O + g_F}{R_Z g_i g_O}(g_i + g_G + g_F)]}] - V_G[\frac{g_G}{[g_F + \frac{g_O + g_F}{R_Z g_i g_O}(g_i + g_G + g_F)]}] \tag{20}$$

Now by converting into resistance from conductances, then,

$$V_O = V_S[\frac{(\frac{1}{R_G} + \frac{1}{R_F})}{[\frac{1}{R_F} + \frac{(\frac{1}{r_O} + \frac{1}{R_F})}{R_Z} r_i r_O(\frac{1}{r_i} + \frac{1}{R_G} + \frac{1}{R_F})]}] - V_G[\frac{\frac{1}{R_G}}{[\frac{1}{R_F} + \frac{(\frac{1}{r_O} + \frac{1}{R_F})}{R_Z} r_i r_O(\frac{1}{r_i} + \frac{1}{R_G} + \frac{1}{R_F})]}] \tag{21}$$

Figure 7 shows a simplified version of the Macro-modelling circuit of Fig6. Moreover; figure 8 represents an analysis model configuration using Norton's theory to alter ($R_z i$) to a current generator.

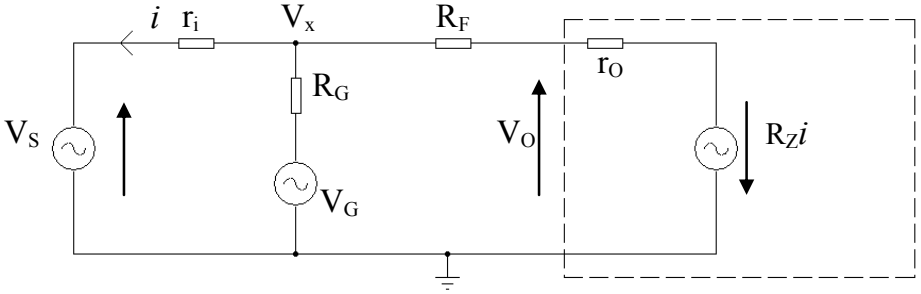

Figure 7: Simplified form of Fig.6

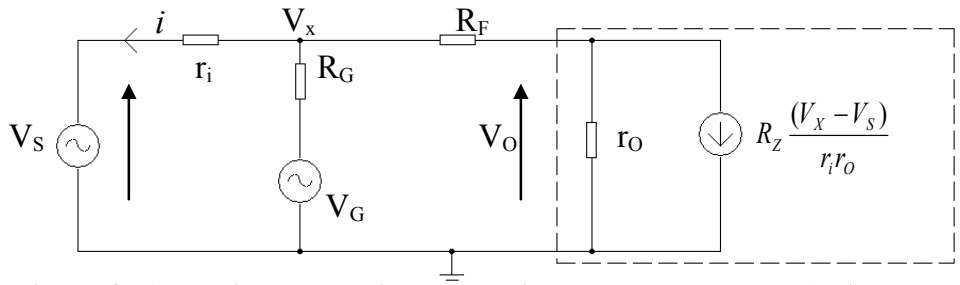

Figure 8: Analysis model using Norton's theorem to change ($R_Z i$) to a current generator

Multiply the numerator and the denominator by ($R_F R_G$),

$$V_O = V_S[\frac{(R_F + R_G)}{R_G[1+\frac{(R_F + r_O)}{R_Z}\left\{1+r_i(\frac{1}{R_G}+\frac{1}{R_F})\right\}]}] - V_G[\frac{R_F}{R_G[1+\frac{(R_F + r_O)}{R_Z}\left\{1+r_i(\frac{1}{R_G}+\frac{1}{R_F})\right\}]}] \quad (22)$$

$$V_O = V_S[\frac{R_F + R_G}{R_G}][\frac{1}{1+\left|\frac{1}{LG}\right|}] - V_G[\frac{R_F}{R_G}][\frac{1}{1+\left|\frac{1}{LG}\right|}] \quad (23)$$

where, by analogy with the conventional voltage feedback operational amplifier, $|LG|$ is the magnitude of the loop-gain (but in this case current loop-gain rather than voltage loop-gain)

$$|LG| = \frac{R_Z}{(R_F + r_O)[1+r_i(\frac{1}{R_G}+\frac{1}{R_F})]} \quad (24)$$

Having $r_i \geq 0$ and $r_O \geq 0$ means a reduced loop gain over that assumed in the conventional first-order treatments of the CFOA in which,

$$|LG| = \frac{R_Z}{R_F} \quad (25)$$

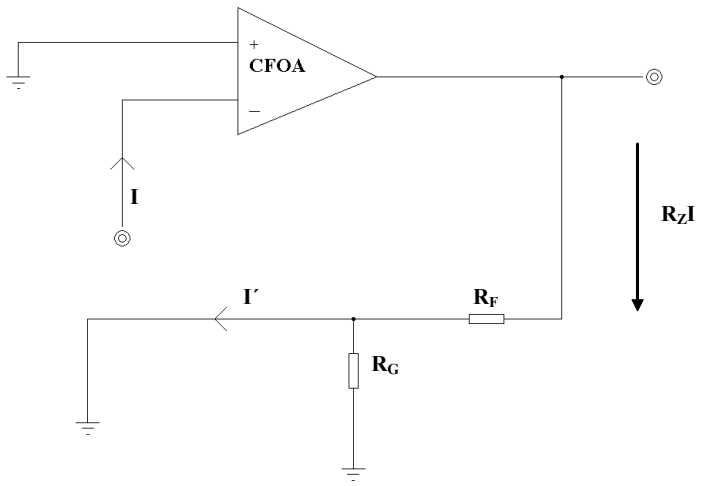

Figure 9: Model for CFOA voltage offset

Figure.9 illustrates a model of the CFOA voltage offset. An interpretation of this is obtained by making $V_S=0$ and inserting a test current I at the inverting input.

$$|LG| = \left|\frac{I'}{I}\right| = \left|-\frac{IR_Z}{R_F}\cdot\frac{1}{I}\right| = \frac{R_Z}{R_F} \quad (26)$$

The analysis so far applies to a.c. inputs but can also apply to d.c. offset voltage. This is taken into account by making $V_G=0$, and inserting $V_S=V_{OS}$

Then, $V_O = \pm V_{os}(\frac{R_F + R_G}{R_G})$ (27)

The ± signs take with account the uncertainty in the direction of V_{os}. The general equation (23), with the assumption $|LG|>>1$, leads to two familiar results:

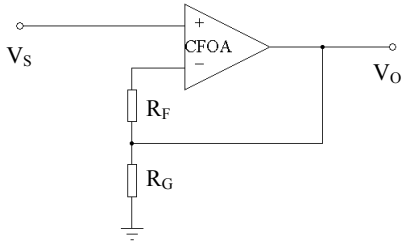

Figure 10: Non-inverting configuration representing equation (28)

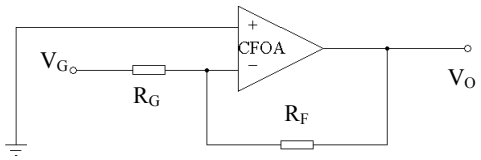

Figure 11: Inverting configuration representing equation (29)

1. $V_O = V_S \frac{(R_F + R_G)}{R_G}$ for V_G=0 (28)

This correspond to the non-inverting mode (Fig.10)

2. $V_O = -V_G \frac{R_F}{R_G}$ for V_S=0 (29)

This corresponds to the inverting mode (Fig.11). However, there is also another result which is obtained by putting V_S=0, and making V_G and R_G very large, but finite, so I_{in}=(V_G/R_G). Then,

$$V_O \approx -I_{in} R_F \quad (30)$$

This is the case of the I/V converter. Figure.12 illustrates an (I/V) circuit configuration for the CFOA

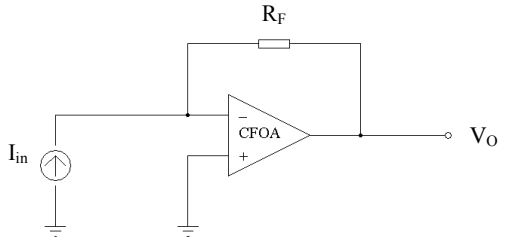

Figure 12: (I/V) circuit configuration representing equation (30)

4. Closed-loop frequency response

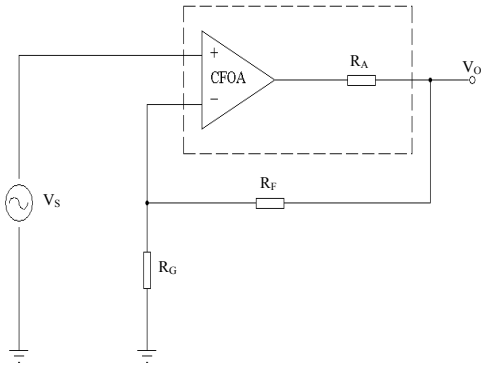

Figure13: Set-up for investigating the effect of r_O on bandwidth

The general expression for CFOA closed-loop amplifier response is,

$$A(o) = \frac{Ideal\ gain}{[1 + \frac{(R_F + r_O)}{R_Z}\left\{1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})\right\}]} \tag{31}$$

This is for low frequencies: to determine the frequency response we must replace ($1/R_Z$) by the $(\frac{1}{R_Z} + sC_Z)$ where s is the complex frequency variable (this assumes all other parameters are frequency-independent: this assumption is examined, further, later) then, the expression,

$$[1 + \frac{R_F + r_O}{R_Z}\left\{1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})\right\}] \tag{32}$$

becomes,

$$[1 + (R_F + r_O)[\frac{1}{R_Z} + sC_Z]\left\{1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})\right\}]$$

(33)

or,

$$[1 + (\frac{R_F + r_O}{R_Z})\left\{1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})\right\}] + (R_F + r_O)sC_Z\left\{1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})\right\}] \tag{34}$$

Hence,

$$A(s)=\frac{Ideal\ \ gain}{[1+\frac{R_F+r_O}{R_Z}\left\{1+r_i(\frac{1}{R_G}+\frac{1}{R_F})\right\}]\left[1+\frac{(R_F+r_O)sC_Z[1+r_i(\frac{1}{R_G}+\frac{1}{R_F})]}{[1+\frac{R_F+r_O}{R_Z}\left\{1+r_i(\frac{1}{R_G}+\frac{1}{R_F})\right\}]}\right]} \tag{35}$$

$$A(s)=\frac{A(o)}{1+\frac{(R_F+r_O)sC_Z[1+r_i(\frac{1}{R_G}+\frac{1}{R_F})]}{[1+\frac{R_F+r_O}{R_Z}\left\{1+r_i(\frac{1}{R_G}+\frac{1}{R_F})\right\}]}} \tag{36}$$

For the usual case $(R_F+r_O)<<R_Z$ it is legitimate to approximate this to,

$$A(s)=\frac{A(o)}{1+s(R_F+r_O)C_Z[1+r_i(\frac{1}{R_G}+\frac{1}{R_F})]} \tag{37}$$

or, in the frequency domain,

$$A(j\omega)=\frac{A(o)}{1+j\omega C_Z(R_F+r_O)[1+r_i(\frac{1}{R_G}+\frac{1}{R_F})]} \tag{38}$$

The (–3dB) cut off frequency occurs when the coefficient of j is unity, i.e. at a frequency f_c given by

$$f_C=\frac{1}{2\pi C_Z(R_F+r_O)[1+r_i(\frac{1}{R_G}+\frac{1}{R_F})]} \tag{39}$$

For the simplest case, assumed in first order treatments, $r_O=0$, $r_i=0$, then,

$$f_C=\frac{1}{2\pi R_F C_Z} \tag{40}$$

However this is only an approximation because, even if r_i is neglected (as $r_i<<R_G//R_F$), r_O cannot be neglected since it may be comparable with R_F for 'low' values of R_F.

$$f_C=\frac{1}{2\pi(R_F+r_O)C_Z} \tag{41}$$

The effect of finite r_i is to reduce the bandwidth to f_c'. The amount of reduction depends on R_G (for a fixed R_F)

$$f_C{}' = \frac{f_C}{[1 + r_i(\frac{1}{R_G} + \frac{1}{R_F})]} \tag{42}$$

To investigate the effect of r_O a simulation SPICE test was carried out using the set-up in Fig.13, in which R_A is an added resistor and the boxed section now represents the modified CFOA. For this arrangement equation (39) should apply with r_O replaced by (r_O + R_A).In the test V_S=100μV (peak) sinusoidal signal. Fig.14, 15, 16, 17, show the frequency response for gain magnitude for values of R_A (0, 150Ω, 1KΩ, –150Ω). To discuss these further we can re-write equation (39) as,

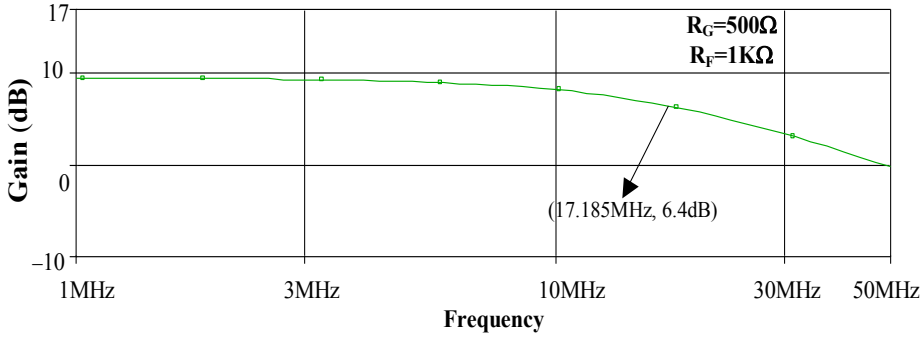

Figure14: CFOA (Bandwidth ~ Frequency) for R_A=0

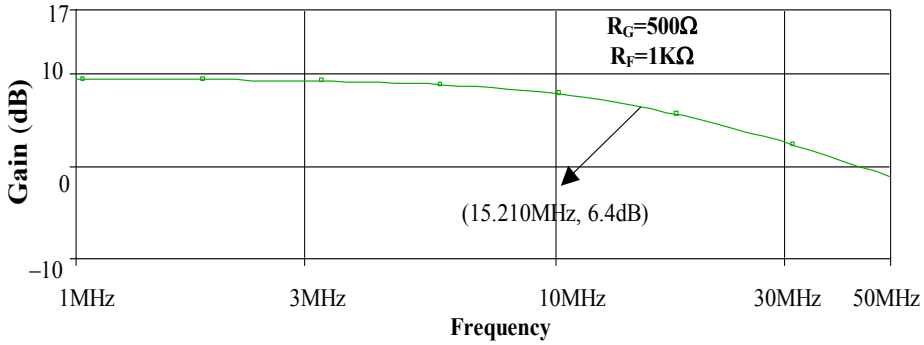

Figure 15: CFOA (Bandwidth ~ Frequency) for R_A=150Ω

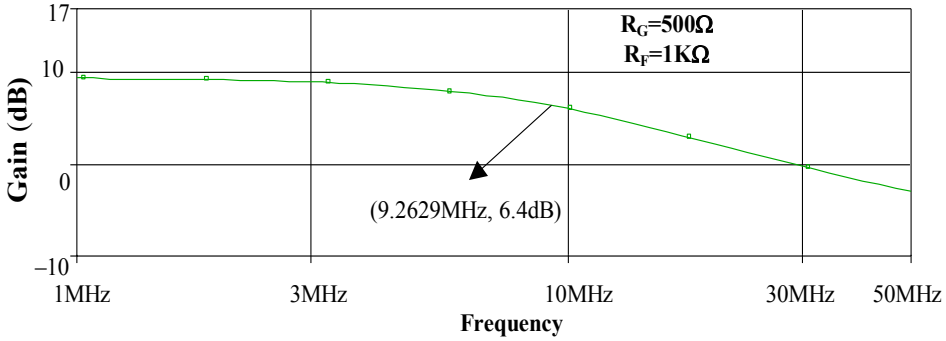

Figure 16: CFOA (Bandwidth ~ Frequency) for R_A= R_F=1KΩ

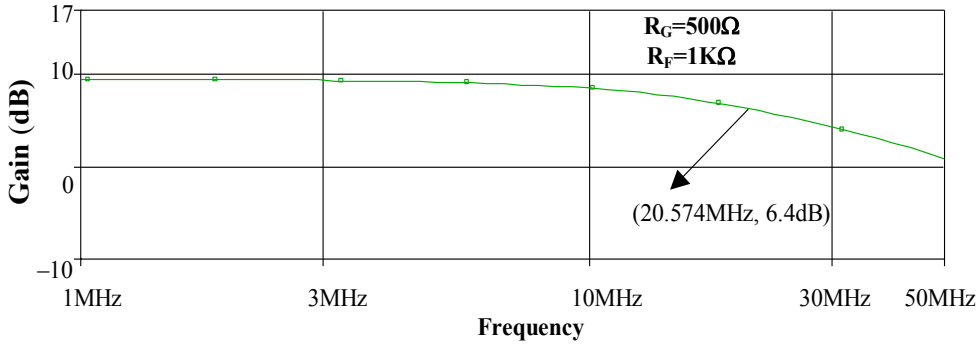

Figure 17: CFOA (Bandwidth ~ Frequency) for R_A= –150Ω

		$R_A(\Omega)$	
		(a)	(b)
f_C (MHz)	Simulated	15.2	20.6
	Calculated	15.3	19.8

Table 1

$$f_C = \frac{K}{(R_F + r_O + R_A)} \tag{43}$$

where K is a constant,
The effective value of r_O can be found by substituting data from Fig.14 (f_C=17.2MHz, R_A=0) and Fig.16 (f_C=9.2MHz, R_A=1KΩ): this gives r_O=0.15KΩ.

Using this value of r_O and the f_C, (R_A=0) of Fig.17 the f_C was calculated for
a) R_A=150Ω
b) R_A= –150Ω

The calculated results displayed in Table 1 are in good agreement with the simulated values. The results suggest an area for further investigation, namely the use of a floating negative resistance to increase f_C. The production of a floating negative resistance in practice is not simple but it has been done and used in the design of precision V/I conversion [26].

Note that R_A has little effect on gain magnitude. This to be expected since r_O in equation (39) only affects a small correction term in the expression for gain magnitude (whereas it has a direct effect on f_C). Counter-intuitively; changing the value of R_A alters the frequency response of the amplifier

In the frequency responses plotted in Fig. 14, 15, 16 and 17 it is shown that the effect of varying R_A over a range from (–150Ω to 1KΩ**)**. Highest when R_A is (–150Ω), with a wide bandwidth of 20MHz. At the other extreme when R_A is (1KΩ), the bandwidth is narrowed to 9MHz.

5. Further observations on the closed-loop frequency response

Since at the inverting input of the CFOA we are looking into the emitters of a complementary emitter-follower stage there is a small inductive component L_i of input impedance at this terminal that has been neglected in this analysis and most previously published analyses. Taking this into account we replace r_i by $(r_i + sL_i)$ in equation (39). Then,

$$A(s) = \frac{A(o)}{[1 + (R_F + r_O)[\frac{1}{R_Z} + sC_Z]\left\{1 + [r_i + sL_i](\frac{1}{R_G} + \frac{1}{R_F})\right\}]} \tag{44}$$

$$A(s) = \frac{A(o)}{[1 + [\frac{R_F}{R_Z} + \frac{r_O}{R_Z} + R_F sC_Z + r_O sC_Z]\left\{1 + \frac{r_i}{R_G} + \frac{r_i}{R_F} + \frac{sL_i}{R_G} + \frac{sL_i}{R_F}\right\}]} \tag{45}$$

For the usual case $(R_F + r_O) << R_Z$,

$$A(s) \approx \frac{A(o)}{[1 + [R_F sC_Z + r_O sC_Z]\left\{1 + \frac{r_i}{R_G} + \frac{r_i}{R_F} + \frac{sL_i}{R_G} + \frac{sL_i}{R_F}\right\}]} \tag{46}$$

By inspection this reduces to the form,

$$A(s) = \frac{A(o)}{[1 + X_1 s + X_2 s^2]} \tag{47}$$

X1, X2 being parameter groupings. In the frequency domain,

$$A(j\omega) = \frac{A(o)}{[1 + j\omega X_1 + j^2 \omega^2 X_2]} \tag{48}$$

It is apparent that the ω^2 term can contribute to peaking in the frequency response which is observed in practice. Of course, the finite frequency response of the current mirrors and the voltage followers, also so far ignored, complicates the matter further.

6. Slew rate

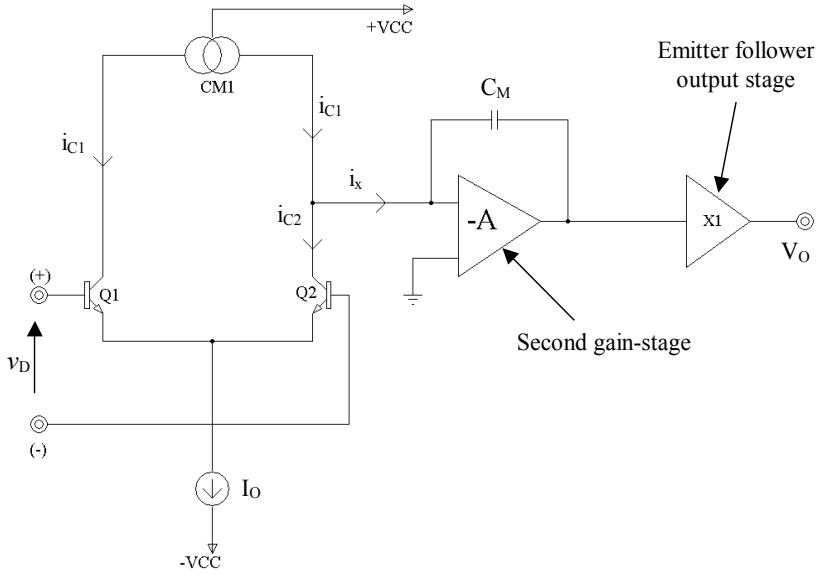

Figure 18: Basic architecture of the VOA

Rise time usually refers to the time it takes for a voltage or current to rise from 10% to 90% of its peak value, and generally this is measured before the onset of large signal limiting due to slew rate. Slew rate limiting is a phenomena generally due to current limitations feeding a key nodal capacitance and is effectively a disconnect between input and output.

The slew rate S, is the maximum rate of change of the output voltage with time when a large-signal step function voltage is applied to the input terminals. The stipulation 'large-signal' inevitably rules out small-signal behaviour. It will be seen that slew rate is limited by the amount of current available to charge a dominant internal node capacitance included to ensure frequency stability under the closed-loop operation. Consider, first, the case of VFOA shown schematically in Fig.18. If v_D is a large positive step-voltage, Q_1 passes the full tail current I_O, so $i_{c1} \approx I_O$ and $i_{c2} \approx 0$. The current mirror CM1 repeats i_{c1}, so the charging current for the Miller capacitance, C_M, included for closed loop frequency stability, is given by, $i_x \approx I_O$.

$$\text{Hence, } S_+ \approx \frac{I_O}{C_M} \tag{49}$$

Similarly, if v_D is a large negative going step-voltage,

$$S_- \approx -\frac{I_O}{C_M} \tag{50}$$

For the VOA type μA741, $I_O \approx 20\mu A$ and $C \approx 30pF$. The resulting value of S is less than 1V/μs. Consider next the case of the basic CFOA, a schematic diagram of which is shown in Fig. 19. The slew rate for this configuration is sometimes quoted as being virtually infinite but definite limits for this do exist as the following brief discussion shows. D_1, D_2 in Fig.19 model the input emitter followers. When a large differential voltage v_D is applied,

in the direction shown, D_1 and Q_2 tend to cut off and the equivalent circuit for discussing slew rate S is that of Fig.20.

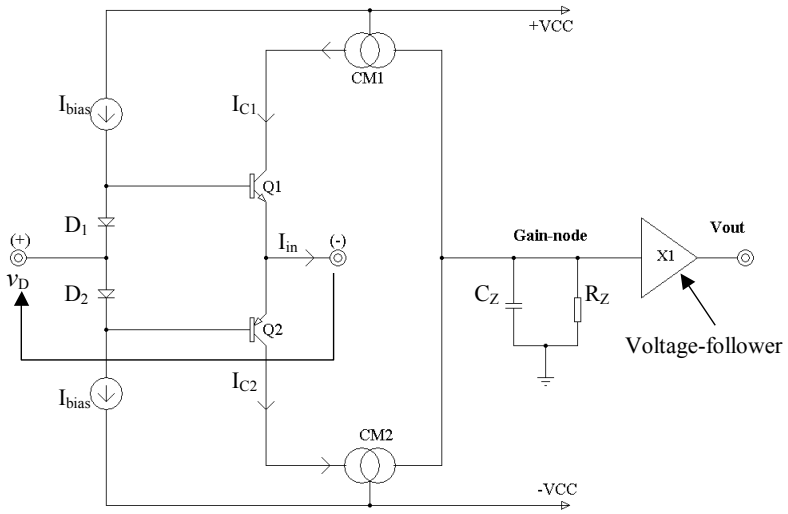

Figure 19: CFOA schematic for slew-rate discussion

thus,

$$S \approx S_+ \approx |S_-| \approx \frac{|I_O|}{C_M} \tag{51}$$

Q_1 is supplied with a step of base current, I_{bias}, that provides a collector current i_{c1}, which can be estimated using transistor charge-control theory [27].

$$i_{c1} \approx \beta_n I_{bias}[1-\exp(-\frac{t}{\beta_n \tau_F})] \tag{52}$$

in which: β_n=c.e. current gain of Q_1 at low frequencies; τ_F is a transistor time-constant dependent on its geometry and doping levels. Actually $\tau_F \approx 1/\omega_T$, ω_T being the characteristic BJT frequency at which $|\beta_n|=1$. The current i_{c1} is repeated by the current-mirror CM1 but i_x is time-related to it. The equation for the voltage rise at point Z is,

$$C_Z \frac{dv_Z}{dt} + \frac{v_Z}{R_Z} \approx \beta_n I_{bias}[1-\exp(-\frac{t}{\beta_n \tau_F})] \tag{53}$$

A limit to slew rate is achieved by setting $\tau_F = 0$ and ignoring R_Z.

$$\text{Then, } S_+ \approx \beta_n \frac{I_{bias}}{C_Z} \tag{54}$$

The same result is achieved for a large negative value of v_D, in which case D_2 and Q_1 tend to cut off. Clearly, for the same operating current ($I_{bias}=I_O$) and capacitor, S is much greater for the CFOA than the VOA. Typical values for the CFOA normally exceed 200V/μs.

The maximum value of the slew rate is obviously achieved with the maximum i_x and highest ω_T, so any improvement over that obtained for the basic CFOA must take these into account. Ultimately the current available from the supplies limits the slew rate and this depends on supply-lead inductance and resistance.

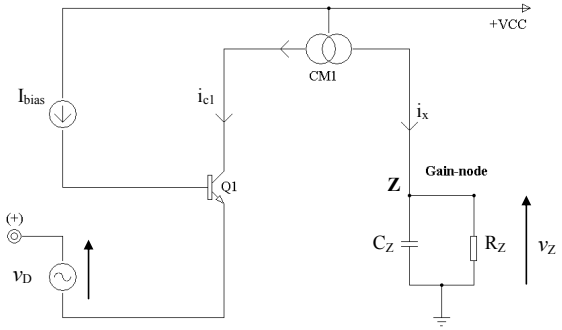

Figure 20: Reduced schematic from Fig.19 for a large v_D

7. Differential and common-mode operation

7.1Differential voltage gain, A_d

Fig.21 shows an appropriate measurement circuit for A_d. R_{F1}, R_{F2} provide d.c. negative feedback, necessary to ensure that the CFOA operates in the linear mode. In the small-signal equivalent circuit of Fig.22, the CFOA is represented by the components within the dashed triangle. If over the test-frequency range C_2 is chosen so that $(1/\omega C_2) << (R_{F1}// R_{F2})$ the ac. feedback is de-activated.

If, furthermore, $(1/\omega C_1) << (R_{in}// R_{F1})$ and $(R_{F2}>>r_O)$, then by inspection,

$$A_d = (\frac{V_O}{V_{in}}) \tag{55}$$

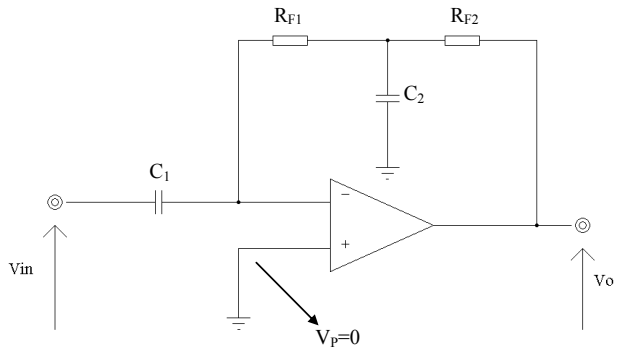

Figure 21: Measurement circuit for A_d

In simulation measurements; R_{F1}=1KΩ; R_{F2}=1KΩ; C_1=1000mF; C_2=1000mF. Figure 23 shown below a reduced form of Fig.22 for large values of C_1, and C_2.

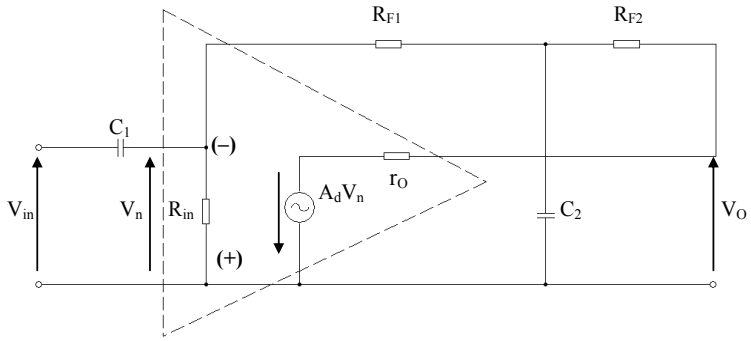

Figure 22: Small signal equivalent circuit

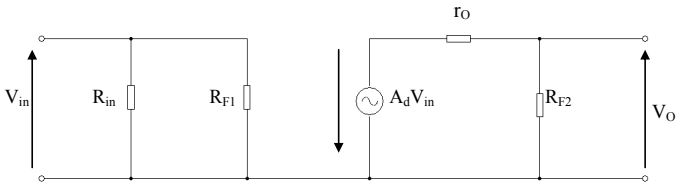

Figure 23: Reduced from of (Fig.22) for very large C_1, C_2

7.2 Common mode gain, Ac, and common mode rejection ratio, CMRR, ρ

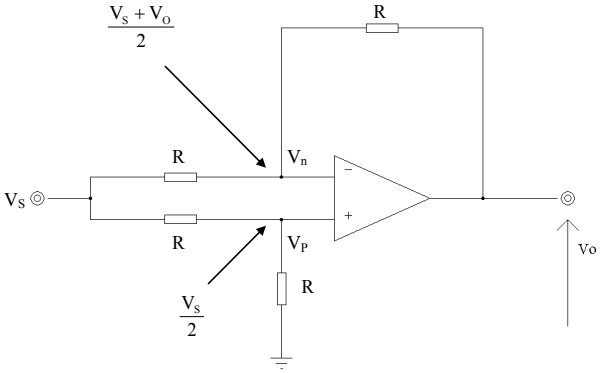

Figure 24: Circuit to find the CMRR, ρ
(In tests, R=1KΩ, V_S=10mV)

Fig.24 illustrates a circuit configuration for determining ρ as far as the CFOA is concerned.

$$V_O = A_d(V_P - V_n) + \frac{A_c(V_P + V_n)}{2} \tag{56}$$

In this Ac is the common-mode gain. But, by inspection, $V_p = \frac{V_S}{2}$ and $V_n = \frac{V_S + V_O}{2}$. Substituting these values in equation (56), [28] gives:

$$(\frac{V_O}{V_S}) = \frac{A_c}{[A_d - (\frac{A_c}{2}) + 2]} \tag{57}$$

Since A_d>>Ac, equation (57) simplifies to equation (58) [29].

$$(\frac{V_O}{V_S}) \approx \frac{A_c}{A_d} \approx \frac{1}{\rho} \tag{58}$$

A knowledge of A_d and A_c in dB permits a determination of ρ which is, otherwise, not easy to determine. By comparison, a practical measurement of ρ, particularly as a function of frequency is somewhat complex. One of these [30] makes use of the fact [31]. Where V_{OS} is the offset voltage, discussed in the next section, and V_C is the common-mode input voltage. The requirement to hold V_O constant is what leads to circuit complexity. It should be noted that the test circuit of Fig.24 is not appropriate for laboratory tests because of the problems of accurate resistor matching [28].

$$\frac{1}{\rho} = \frac{\partial V_{OS}}{\partial V_c}\Big|_{V_O} \tag{59}$$

8. Input offset voltage, V_{OS}

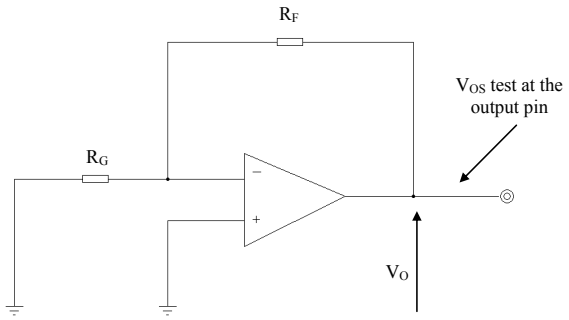

Figure 26: Voltage offset test circuit

Ideally, the d.c. output voltage of a CFOA, like that of a VOA, should be zero when differential input voltage is zero [32]. However, because of slight imbalances in the amplifier the output voltage of a real CFOA is not zero when the input terminals are at the same potential (normally, earth potential) [29]. The magnitude of the voltage that must be applied between the input terminals to reduce the output voltage to zero is the input offset

voltage (or, differential input offset voltage), V_{OS}. Since it is normally quite small, e.g. a few milli volts, measurement of it under laboratory conditions are normally achieved by using the CFOA itself to amplify it. The circuit for this is shown in Fig.26, which is also used in PSPICE analysis.

It can be shown that subject to normally easily-met parameter relationships [29],

$$V_{OS} = \pm \frac{V_O}{A_{CL}} \tag{60}$$

where A_{CL}= magnitude of closed loop d.c. voltage gain or, $A_{CL} = \frac{(R_F + R_G)}{R_G}$. The plus and minus sign allows for the possibilities of the imbalances. Table 2 show convenient test choices.

R_G	R_F	Gain	Offset voltage V_{OS}
1KΩ	10KΩ	11	$V_{OS} \approx \pm \frac{V_O}{11}$
1KΩ	5KΩ	6	$V_{OS} \approx \pm \frac{V_O}{6}$
1KΩ	1KΩ	2	$V_{OS} \approx \pm \frac{V_O}{2}$

Table 2 Finding V_{OS} from V_O for the circuit of Fig.26

9. Unity-gain frequency response

This is a small-signal parameter that defines the frequency at which the a.c. gain is 3dB down its d.c/low frequency value [33]. It is normally measured with the CFOA connected as a voltage-follower (see Fig.27): a parallel R, C load reduces output noise.

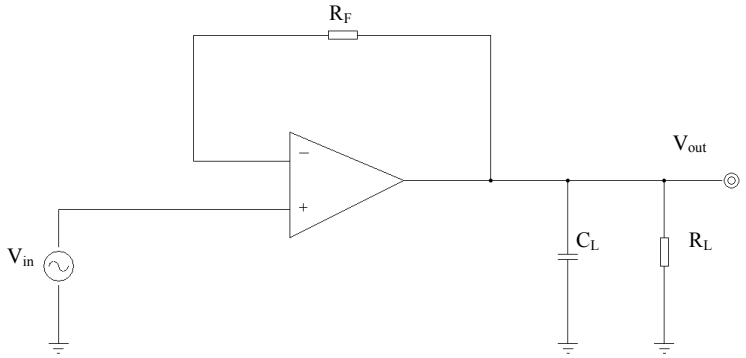

Figure 27: Frequency-response measurement circuit

The a.c. unity-gain error is:

$$\varepsilon = (\frac{V_{out} - V_{in}}{V_{in}}) \tag{61}$$

Fig.28 shows how it is determined from simulation.

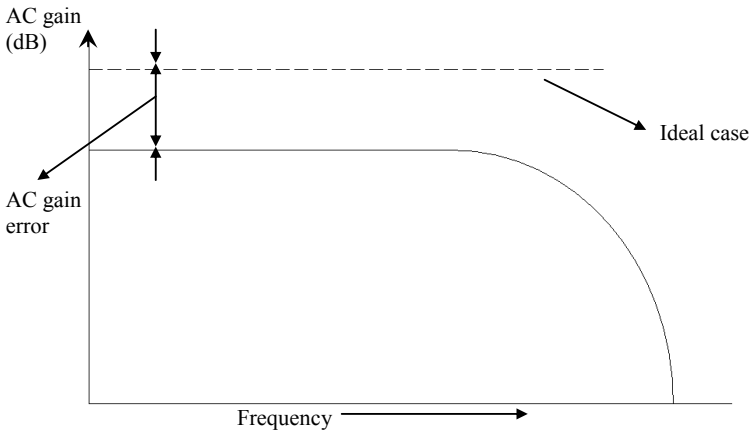

Figure 28: Definition of a.c.-gain error

10. Slew Rate testing methodology

This is a large-signal parameter. It defines the magnitude of the maximum rate at which the output voltage can change when a large signal voltage is applied to the input. It is expressed in V/μs [34].

As in the measurement of the frequency response, the CFOA is connected in the voltage–follower configuration (Fig.29). A rectangular voltage test pulse of amplitude V and rise and fall times t_{ir}, t_{if} is applied to the input (Fig.30 a). The resulting output rise and fall times are t_{or}, t_{of}, respectively. The slew rate in the positive-going edge is S_+, where,

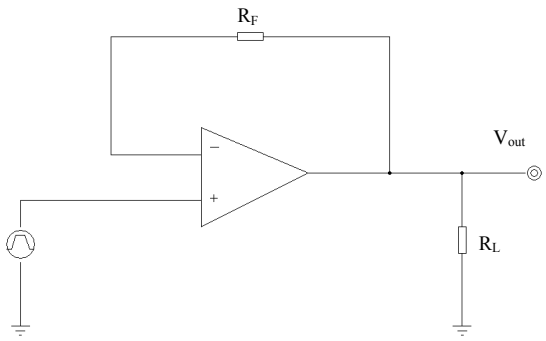

Figure 29: Slew rate measurement circuit

$$S_+ = \left| \frac{dV}{dt} \right| = \frac{V}{t_{or}} \tag{62}$$

That for negative-going edge is S_-,

$$S_- = \frac{V}{t_{of}} \tag{63}$$

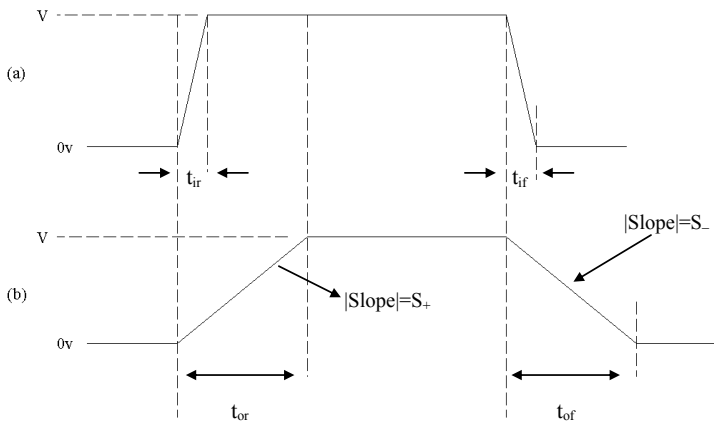

Figure 30: Waveforms for Fig.29

$$f_p = \frac{S}{2\pi \hat{V}_{in}} \tag{64}$$

Since these two parameters may differ, the smaller is taken as defining the slew-rate. To determine if 'large -signal' conditions apply V can be increased. If S_+, S_- do not change, then V is 'large' enough. Similarly to determine if t_{ir}, t_{if} are sufficiently small in comparison with t_{or}, t_{of} (so they do not play a part in determining) them, t_{ir}, t_{if} can be doubled. If S_+, S_- do not change then t_{ir}, t_{if} are sufficiently small. A good measurement choice is $t_{ir} \leq$ (expected t_{or})/10 and $t_{if} \leq$ (expected t_{of})/10.

Related to S is the full-power bandwidth fp.

11. Input impedances

11.1 The non-inverting input impedance

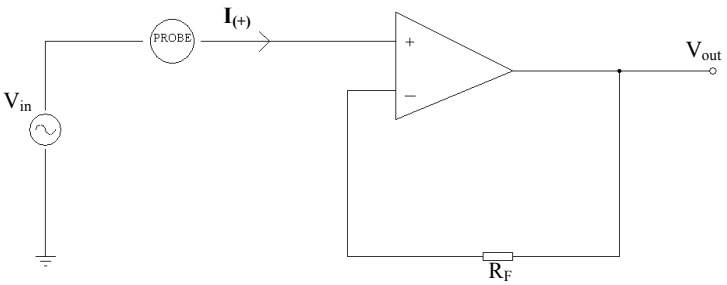

Figure 31: Test circuit for non-inverting input resistance

The input impedances of the VOA are the normally the same at each of its two input terminals because the latter is based on an emitter coupled pair input stage. However, this is

not the case for the CFOA because of its different architecture. The CFOA has a complementary-pair input stage as a replacement to the traditional long–tail pair input design. This means that a slightly different measurement technique has to be used for the two inputs.

The magnitude of the input impedance, as a function of frequency, looking in at the non-inverting input of the CFOA is conveniently measured by connecting the amplifier to operate as a voltage-follower with a d.c. input bias voltage of zero volts. A small amplitude voltage signal V_{in} of variable frequency, is applied at the non-inverting input and the resulting input current, I_{+}, measured (Fig.31)

Then, $$| Z_{i(+)} | = \frac{V_{in}}{I_{+}} \quad (65)$$

From a plot of $|Z_{i(+)}|$ versus frequency, the input impedance can be interpreted as a parallel combination of resistance and capacitance.

11. 2. Inverting input impedance

Fig.32 shows a convenient test circuit for measuring the magnitude, $|Z_{i(-)}|$, of the impedance looking in at the inverting input terminal. As in the case of the measurement of $|Z_{i(+)}|$, V_{in} is a voltage signal of variable frequency, but now V_{in} is reduced in amplitude by the presence of R_G, R_F. This is necessary because V_I, the potential difference between the input terminals must be small to limit the magnitude of $I_{(-)}$.

$$| Z_{i(-)} | = \frac{V_I}{I_{-}} \quad (66)$$

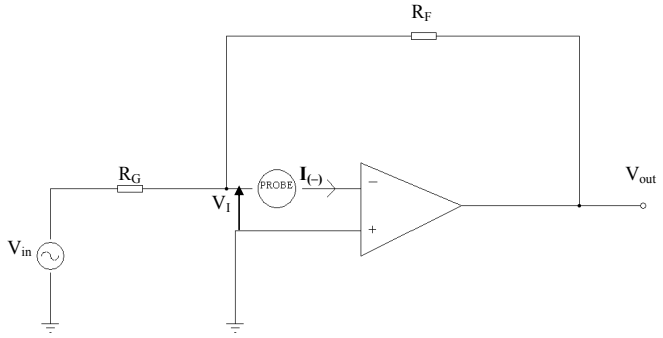

Figure 32: Test circuit for the inverting input impedance

12. Z-point impedance

The circuit of Fig.33 was used to obtain simulation results for the open-loop output impedances of the current-mirror section of the CFOA (i.e. Z-node). This determines the transimpedance of the CFOA, and also has a direct effect on the output impedance of the amplifier. A sinusoidal signal, V_x, of 0.1V peak amplitude is applied, as shown, when the d.c. bias level of the current-mirror output is zero. This ensures that the current-mirrors operate in the linear region. The resulting current, I_x, is measured then output impedance is given by the ratio V_x/I_x. The magnitude of this ratio is plotted as a function of frequency.

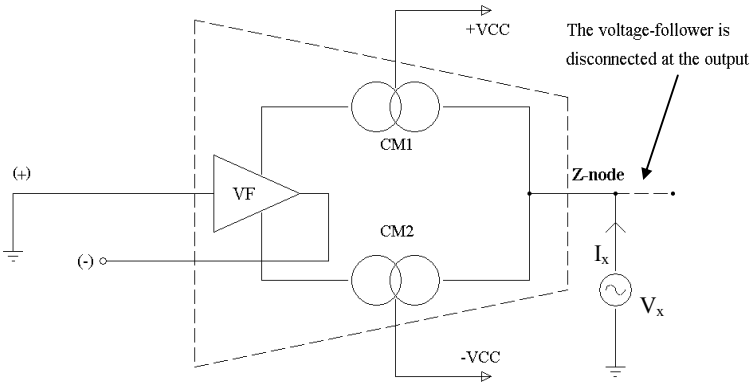

Figure 33: Measuring the output resistances at Z-node

13. Open-loop output resistance, r_O

The measurement of open-loop output impedance and, hence, output resistance, r_O, presents some difficulties [35]. Referring to Fig.33, if the non-inverting input of the CFOA is earthed and there is no feedback, the high output resistance of the two current-mirrors causes the Z-node to assume a potential corresponding to the simulation voltage of either CM1 or CM2, depending on whether the output current CM1 (nominally equal to that of CM2) is greater or less than that of CM2.

To overcome this problem it is necessary to apply at Z-node a direct current, from an infinite impedance source, of such a magnitude and direction as is required to restore the d.c. voltage at Z-node to zero. The output impedance of the CFOA is then found by applying a small current change at the output of the voltage follower, observing the resulting voltage change, and forming the appropriate ratio

14. Conclusion

An op-amp that has a non-linear effect can cause a degradation in input referred noise and slew rate performance. This paper looked at the theoretical study of the slew rate and evaluation of the architectural differences between the conventional VOA, and the conventional CFOA in order to fully understand how op-amps behave dynamically. In the VOA, when a sinusoidal waveform is applied to the input, the output is expected to be a reproduction of the shape of the input signal. Unfortunately, this is not the case due mainly to the fact that the VOA architecture provides inherent limitations in the slew rate. The design of the input stage of the VOA is a transconductance block with a classical long-tail pair input. The VOA topology shows a compensation capacitor C_Z, and high impedance node where the voltage gain is produced. Now the transconductance of the VOA is slew-rate limited due to the current available to charge or discharge C_Z which is the bias current (I_{bais}=Io) of this stage. The transconductance of the VOA will obviously provide an output saturation level, which causes limited slew-rate capability. As a result, an output waveform is distorted by this effect, and the amplitude will be reduced.

The theoretical absence of slew-rate limiting is one of the CFOA's attractive features. This arises from the fact that the maximum current, I_O, available to charge the internal capacitance C_Z, at the onset of a step is proportional to the step, regardless of its size. The time constant ($\tau \approx C_Z R_F$) must be constant. The slew rate of a current feedback op-amp will only be finally limited by the maximum value of the current drive into the base of the transistors, which is set by the (I_{bias}) current value. A high slew rate is obtained as a result of using the current as a feedback error signal. Slew-rate limiting is a major cause of high-frequency distortion in high frequency amplifiers that are handling the output signal levels. In this paper, the theoretical study indicates that in the CFOA, the non-saturation transconductance (g_m) provides a theoretically unlimited slew-rate capability, so that the CFOA gives low distortion for large amplitude, high frequency inputs. In practice, the slew-rate is governed by the power-supply's ability to deliver sufficient current to the class-AB complementary pair, and by the power dissipation in the circuit.

The CFOA exhibits an almost constant closed-loop bandwidth for closed-loop voltage gains. The critical study in this paper shows that it is necessary to set both the closed-loop bandwidth R_F and to set the gain R_G. A typical value for R_F would be between (750Ω to 2.5KΩ), as CFOA manufacturers recommend. The results again show the unique feature of the CFOA design, which has made the bandwidth remain constant as a function of the closed-loop gain. In CFOA, the designer must be careful in deciding how to use a reactive feedback element (such as in the case of the integrator operation), because the closed loop pole must be lower in frequency than any reactive component poles when it is connected directly from the input to the output, in order to insure stability in the closed-loop operation for all gain settings. Otherwise, if the designers are not careful, the domain pole can be shifted too close to the secondary pole, and oscillation might occur as a result. These characteristics are due to the CFOA asymmetric class-AB input stage, which make it a very suitable amplifier for video signal processing. The theoretical performance of the CFOA in terms of bandwidth has been looked at and the author has suggested that the effect of the output impedance on the bandwidth could be further investigated by future researchers. This paper also consider techniques for the measurement of key parameters of the CFOA: PSPICE simulation software was developed for this purpose.

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