# A two-stage opamp frequency Compensation technique by splitting the 2nd stage

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***Abstract*—In this paper miller compensation of opamp has been explained intuitively and discussed the problems existing with this traditional way. Proposed an area/power efficient technique by splitting the second stage has been proposed. The splitting introduces an extra zero in the transfer function such that it will improve the stability. This tech was implemented in 45nm CMOS technology and simulated with Spectre. Simulation results show that the proposed circuit saves 50% of the capacitance area compared to the miller technique. The circuit draws 320uA current from 1.5V supply and occupying 0.003108mm2 silicon area.**

**Keywords—Opamp, Miller, capacitor, Pole, Bandwidth, phase margin, noise.**

## I. INTRODUCTION

The present electronic systems greatly depend on the performance of the amplifier. Both high gain and high bandwidth while consuming very low power are the primary design goal. With the ever-decreasing size of transistors due to technology scaling, the internal electric field of the junctions has been increased greatly which creates all short channel second-order effects like Drain induced barrier lower (DIBL), channel length modulation etc [1]. To combat the second order effects devices researchers have been forced to decreased decreasing the supply voltage, thus the voltage gain and output swing of the amplifiers are greatly decreased. Fig. 1 shows how the voltage gain of a single stage amplifier decreases with the technology, due to velocity situation and channel length modulation, the gain has been decreased by less than 10 around 28nm technology. Another difficulty with the scaling is exponential increase in the leakage current through the gate and drain to substrate junction leakage. Gate leakage current is strongly depending on the thickness of the $Sio_2$ oxide and this has been decreasing with technology scaling and currently, it is in the order of few nm in 65nm [2]. To reduce the leakage while keeping the oxide thickness same as proposed, threshold voltage ($V_{th}$) has been kept or decreased with much lesser pace compared to the supply voltage ($V_{dd}$). Fig. 1 also shows how the $V_{dd}$ is decreasing with the technology. But unfortunately, higher $V_{th}$ for a given $V_{dd}$ reduces the signal swing for a given power dissipation. Generally, sensor or bio-medical application requires 80dB to keep the settling error less than 0.1%.

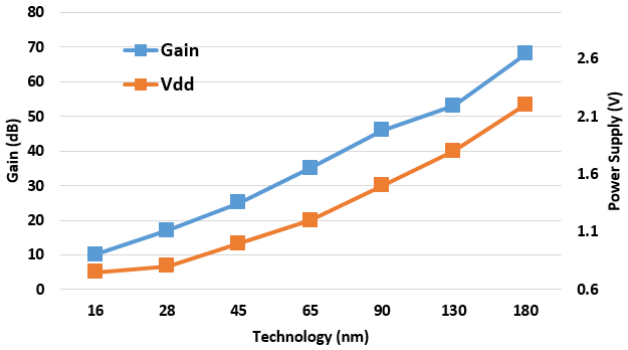


Fig. 1. Gain vs Technology Node

Conventional telescopic or folded Cascode amplifiers, which increases the gain by stacking up transistors is a good technique to increase the gain but at the cost of increased power supply voltage. Or for a given supply the output swing is getting decreased. Often multistage amplifier is a widely used technique to enhance the voltage gain by cascading the number of gain stages horizontally. In this way, circuits can compatible with the low voltage technologies and give acceptable voltage gain. For example, two-stage operation amplifier is very popular in both industry and academia, which achieves very high gain as well acceptable output swing by using a Common Source amplifier as a final stage. This popularity is because of its un-conditionally stable nature irrespective of the feedback factor and load capacitance, hence it can be used as general purpose opamp [2]. However, multistage amplifiers are needed to get higher gain even though the voltage gain is decreasing with technology scaling. Each stage contributes one low-frequency pole in the overall transfer function hence several low-frequency poles in the multi stage combination will leads to un-stable amplifier in the closed-loop configuration. Usually, instability gives peaking in the frequency response and ringing in the time domain and compromises the performance. Often frequency compensation is essential for stable operation, which consumes higher power and silicon area to place the compensation capacitor [3]. This motivates to find an area and power efficient compensation technique.

The rest of the paper has been organized as follows. Section II reviews the existing miller compensation intuitively and design guidelines, Section III explains the proposed technique qualitatively as well quantitatively and section IV summarizes the prototype results.

## II. REVIEW OF MILLER COMPENSATION.

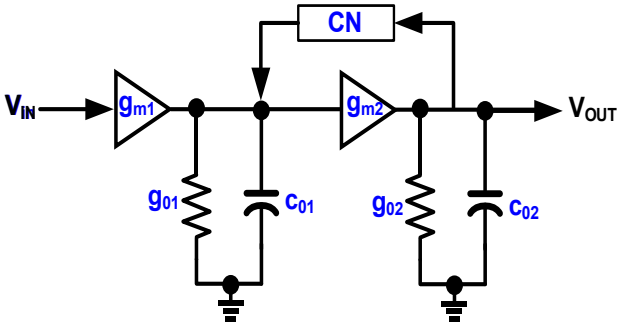


Fig. 2. Conventional Miller Compensation Model

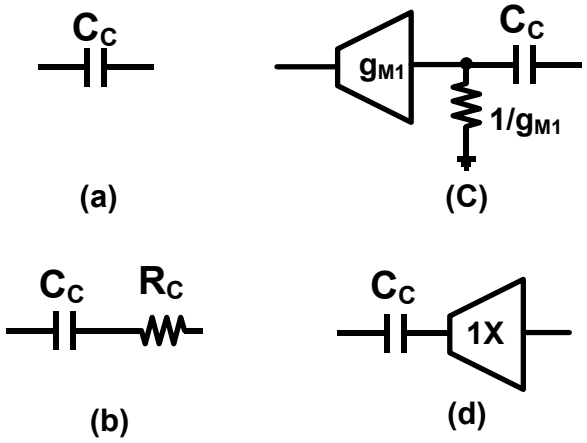


Fig. 3. Conventional Compensation-Network (CN) circuits

Fig. 2 shows the conventional two-stage miller compensation, where the first stage is a typical single stage opamp with the high impedance active load, whereas common source as the second stage. A compensation network (CN) consists of resistor and capacitor will be generally added to compensate the system for improved stability. There have been four types of the CN's as shown in fig. 3. (a) shows Simple miller compensation (SMC) with a simple capacitor as CN, (b) shows SMC with a Zero nulling resistor whose value equal to $\frac{1}{gm_2}$, (c) shows SMC with a current buffer to push RHP to very high frequency and (d) shows SMC with a voltage buffer. Without any compensation network opamp dominate pole at $\frac{1}{R_{01}C_{01}}$ and non-dominate pole at $\frac{1}{R_{02}C_{02}}$. Fig. 4 depicts the small signal model of the miller compensation. The compensated (means capacitor as a feedback element) the opamp transfer function can be written as

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m2}\left(1-\frac{SCc}{g_{m2}}\right)}{AS^2+BS+C} \qquad (1)$$

Where $A=c_{01}c_c+c_{01}c_{02}+c_{02}c_c$
$B=c_c(g_{m2}+g_{02}+g_{01})+c_{02}g_{01}+c_{01}g_{02}$ and $C=g_{01}g_{02}$

By using wide pole separation Closed loop poles can be written as

$$P_1 = \frac{g_{01}}{C_C\left(\frac{g_{m2}}{g_{01}}+1+\frac{g_{01}}{g_{02}}\right)+C_{01}+C_{02}\frac{g_{01}}{g_{02}}} \qquad (2)$$

$$P_2 = \frac{g_{02}+g_{m2}\frac{C_C}{C_C+C_{01}}+g_{01}\frac{C_C+C_{02}}{C_C+C_{01}}}{C_{02}+\frac{C_CC_{01}}{C_C+C_{01}}} \qquad (3)$$

From the above two equations it is evident that dominate pole frequency ($P_1$) has been decreased and non-dominate pole frequency ($P_2$) went high. For this reason, Miller compensation will also be known as pole-splitting compensation. Almost every researcher has shown the math's to show the splitting but there is no intuitive explanation why poles do so [4]. Looking at the fig.2 it is clear that miller capacitor will be multiplied by the -ve gain of the second stage hence the load capacitance seen by the first stage will be increased by $g_{m2}*r_{02}$ times and $P_1$ will move down. Whereas at high frequency, the impedance looking at the output of the second will increases a lot, because of the feedback formed by the $C_C$ and $C_{01}$. Effective impedance has decreased and pole frequency went up. The approximate location P2 can be expressed as (4).

$$P_2 = \frac{g_{m2}}{C_L}\frac{1}{1+\frac{C_{01}}{C_C}} \qquad (4)$$

This indicates that the total amount of phase shift introduced by the loop has decreased by the ratio of the final pole locations. Also, this technique has increased the system bandwidth considerably compared to the dominant pole compensation because $P_2$ frequency increased [3].

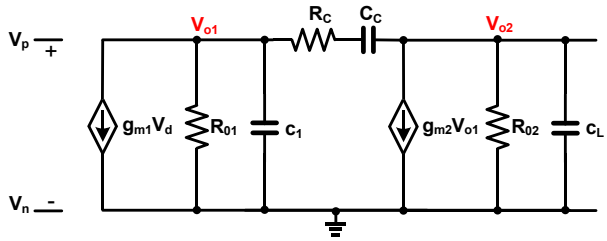


Fig. 4. Small signal model of the miller technique

## III. PROPOSED COMPENSATION TECHNIQUE.

In the past, although various miller compensation schemes have been proposed to improve the gain bandwidth product, complexity also increased interims of additional amplifier stages and capacitors [3-10]. Miller compensation with a nulling resistor introduces a right half zero (RHP) which compromises the stability. Ahuja [5] and [6] proposed a current buffer in series with a compensation capacitor to cancel RHP, the downside of this technique is complex poles in the closed loop. A damping stage based compensation proposed in [3]- [5], but the technique has poor power supply rejection (PSRR). [8] has proposed cascade compensation, by connection compensation capacitor at a low impedance node to eliminate RHP zero, often creating a low impedance node with-in the Opamp demands a lot of power. The downside of

existing miller technique is the excessive power consumption in the second stage because, for a given compensation capacitor, 2nd $g_m$ should be chosen such that second dominate pole should 2-3X higher frequency relative to the Unity Gain Bandwidth (UGB). Typically, second stage load capacitance will be decided by the preceding stage, hence the only one variable to adjust is the second stage $g_m$, unfortunately this will cost us significant power. [7] proposed feedforward technique to improve the stability by adding another parallel stage such that zero would be formed near UGB, this is having serious settling problems. [9] proposed a split length technique to improve the stability but at the cost of the split devices.

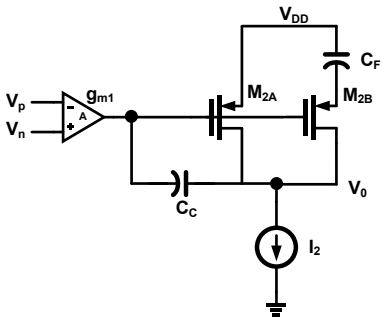


Fig. 5. Proposed compensation technique.

Fig. 6 shows the proposed concept of the compensation, basically the second stage has been split into two parts, $M_{2A}$ transistor carries bias current for linearity requirements, whereas $M_{2B}$ transistor capacitively coupled such that it won't draw any current. At high frequency means beyond the unity gain bandwidth of the opamp, $C_F$ offers low impedance such that the second stage $g_m$ is $g_{m2A}+g_{m2B}$, hence second stage pole has been moved to a high frequency which results in better phase margin [7]. The approximated equivalent second stage $g_m$ frequency response can be expressed as follows.

$$G_{m-second} = g_{m2A} + \frac{g_{m2B}}{1+\frac{g_{m2B}}{SC_F}} = g_{m2A}\frac{1+SC_F\left(\frac{1}{g_{m2A}}+\frac{1}{g_{m2B}}\right)}{1+\frac{SC_F}{g_{m2B}}} \quad (5)$$

(5) Reveals high-frequency pole compared to the existing one, here $g_{m2A}/g_{m2B}$ plays a significant role. Careful adjustment of the series capacitor ($C_F$) with $M_{2B}$ improves phase margin by $24^0$. With the traditional technique to improve phase margin by this amount second stage current needs to increase by 1.19 times, hence this technique saved 19% of the second stage current. The other important aspect of the opamp is not effected by the proposal like slew rate, input referred offset [10]. Slew rate depends mainly on the first stage bias current and compensation capacitor hence not affected by this as long $M_{2A}$ current is higher than first stage current (which is a typical scenario).

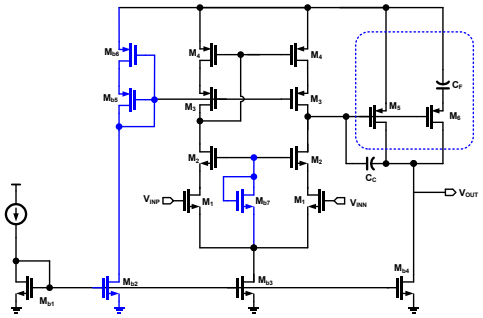

Fig. 6. Implementation of the proposed Technique.

## IV. Simulation Results

To demonstrate the efficiency of the proposed technique, it has been implemented in 8-metal and 1-poly standard 45nm CMOS technology and traditional miller compensated opamp also been implemented for comparison purpose. The targeted gain of the amplifier is 80dB in the typical process and at room temperature. It draws 320µA current from 1.5V supply voltage. The total capacitance required to composite the opamp is only 750fF, whereas the miller technique requires almost 1.6pF, which reveals that proposed technique saved 50% of the capacitance. Fig.7 shows the dc transfer characteristics of the opamp with differential input on the X-axis and the output voltage on Y-axis. The slope around the zero-differential voltage will give a reasonable estimate of the gain, as shown in fig it is ~10000. Such a high gain is because of the cascode stage in the first stage and they have been biased in the weak-inversion region. Fig.8 shows the open-loop frequency response (magnitude as well as phase), which shows 80dB loop-gain at low frequency, 2MHz unity gain bandwidth (UGB). The Phase margin (PM) in the unity gain configuration is 500, which is sufficient to have ringing less closed-loop step response. Input referred offset is a very critical parameter for sensor application, as it compromises the sensitivity of the sensor. The typical acceptable offset is maximum of 2mV. Fig. 9 shows the simulated input referred offset, with a mean of 0mV and sigma of 0.45mV. With-in 3sigma distribution, the achieved offset is 1.35mV.

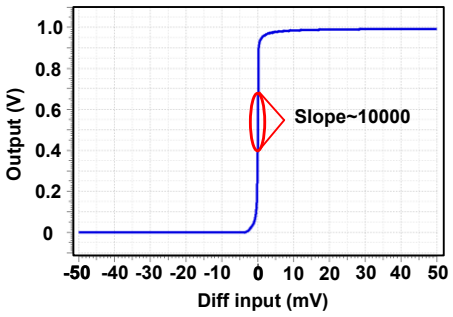


Fig. 7. Dc transfer characteristics.

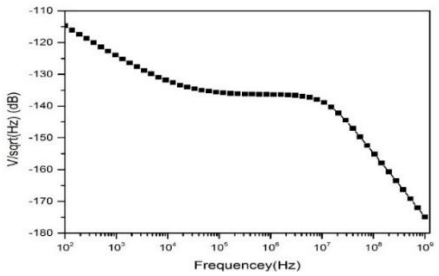


Fig. 8. Simulated input referred Noise PSD.

Fig. 10 shows the noise PSD of the compensated amplifier, it shows -140dB at the bandwidth and integrated noise around the frequency band is 1.2µV.Fig. 11 shows the model layout of the proposed circuit. It occupies 74um*42um silicon area. Every transistor has been laid with proper care towards Mismatch. Special care has been taken for well proximity effect (WPE) and Shallow trench isolation (STI), by adding enough dummies for each device and keeping MOSFET away from NWELL [11].

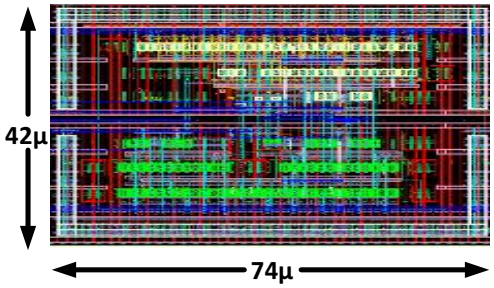


Fig. 9. Layout of the circuit.

## V. Conclusion

In this paper, an area efficient opamp compensation technique has been proposed and validated with the simulation results. Demonstrated 50% saving in the capacitance area. Post layout simulations show 80dB dc gain and 2MHz bandwidth and require 750fF capacitor to achieve $50^0$ Phase margin. Circuit occupies 0.003108mm$^2$ silicon area. Implemented in 45nm CMOS and circuit draws 320uW while powered from 1.5V Power supply.

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