Wide-Bandwidth CFOA with High CMRR Performance

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Abstract

In this paper the authors analyse the conventional current-feedback operational amplifier (CFOA) in terms of common-mode-rejection ratio (CMRR) performance, and having identified the mechanism primarily responsible for the CMRR, they propose two new architecture CFOAs. These new CFOAs are further developed, and modified to provide improved bandwidth, AC gain accuracy and high CMRR performance. The key features of the two proposed new CFOAs are the designs of the internal voltage followers which have two separate biasing currents with a similar dynamic architecture to that of the conventional CFOA. The magnitude of one bias current determines the value of the maximum CMRR, and the second can be used to maximise bandwidth.

Keywords: (CFOA; CMRR; Bandwidth; Input referred offset voltage; Slew-rate; VOA, DAC/ADC buffers, Medical applications)

1. Introduction

In electronic circuit design, there are many occasions where a general-purpose voltage operational amplifier (VOA) is useful [1]. If the application calls for differential inputs, high input impedance, low output impedance, high common-mode rejection ratio **(**CMRR**)**, and low input referred offset voltage, the VOA provides a basic topology for achieving these requirements [2]. Unfortunately it has inherent limitations in both the gain-bandwidth trade-off and slew-rate [3]. Typically, the gain-bandwidth product is a constant and the slew-rate is limited to a maximum value determined by input stage bias current. The slew-rate limitations of the VOA are overcome in relatively new architecture op-amps, commonly referred to as the current-feedback op-amp (CFOA) [4], and [5]. CFOAs have been around approximately 30 years, but their popularity has increased only in the last 10 years. CFOAs are receiving increasing attention as basic building blocks in analog system design, and they are now recognized for their excellent performance in high speed and high slew-rate analog signal processing applications [6]. Despite excellent high frequency and high speed performance, CFOAs generally exhibit poorer common-mode rejection (CMRR) properties, compared with their voltage-mode counterpart, which limits their utility [7].

Electronics manufacturers and telecommunications systems engineers are endeavoring to achieve the highest specifications for a voltage follower [8]. The differential pair is inherently good in providing high CMRR. However, applications such as DAC/ADC buffers, high-quality video front-end, RF/IF drivers, ATE pin drivers, video-line drivers, some medical applications and video switchers showed that having high CMRR, and low DC voltage offset was not enough [9], and [10]. The need for a high-slew-rate voltage follower with a high bandwidth, and low settling-time is desirable for such applications [11], and [12]. In this paper the authors analyse the conventional CFOA and identify the main reasons for the poor CMRR performance. These results were used to inform the development of a new architecture design which addresses the shortcomings in terms of CMRR and gain accuracy. The two new voltage followers proposed in this paper maintain both high slew-rate and good CMRR performance.

2. Analysis of differential-mode operation

A detailed analysis of the input stage is presented in this section to obtain a clear understanding of the operation of the amplifier and gain insight into ways that the circuit can be modified to improve its performance. A simplified schematic of the standard CFOA architecture is shown in Fig. 1 where the non-inverting and inverting nodes are connected to a differential input signal V_2 and V_1 respectively. The positive differential input signals are $V_2 = +\frac{V_{in}}{2}$ and the negative differential input signal is $V_1 = -\frac{V_{in}}{2}$. When the positive signal (V_2) is applied, the voltage at the base of Q_1 will rise, and the voltage at the emitter of Q_1 will fall due to the negative signal (V_1), increasing V_{BE1} of Q_1 and resulting in an increase of I_{C1}. Similarly, V_{BE2} of Q_2 decreases and I_{C2} reduces. Under small-signal the collector current I_{C1} of Q_1 will rise by ΔI and, similarly, the collector current I_{C2} of Q_2 will fall by ΔI [13]. Currents I_{C1} and I_{C2} are then mirrored by CM1 and CM2 to a high impedance gain-node (Z), where they subtract, giving a total signal current $I_Z = 2\Delta I$, resulting in an output voltage $V_{out} = 2\Delta I\ Z_Z$.

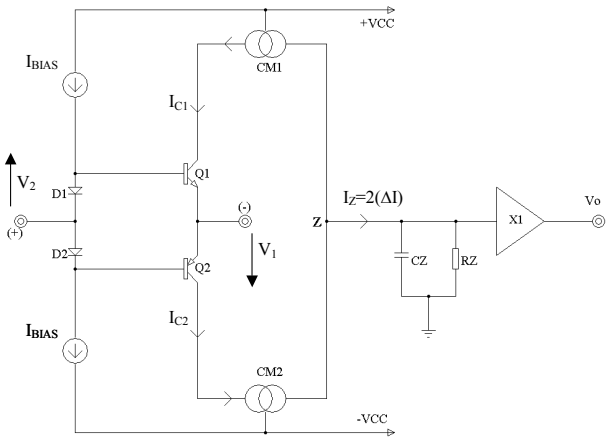

Fig. 1. Simplified schematic of a standard CFOA.

Transistors Q_1 and Q_2 are configured as a class-AB complementary-pair stage. The operating point of these transistors is in the active region and class-AB with the DC current set by the bias network comprising the two diodes D_1 and D_2 and the two current sources, I_{BIAS}.

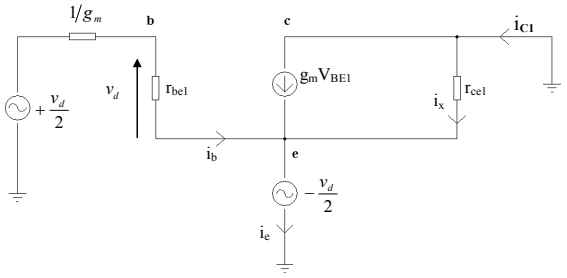

Fig. 2. Small-signal differential-mode half circuit.

Fig. 2 shows the small-signal differential-mode half circuit, which can be analysed to predict the circuit behaviour. $V_d = V_2 - V_1$. The output current $i_{C1} = i_{out(dm)}$ is given by

$$i_{C1} = g_m V_{BE1} + \frac{v_d}{2r_{ce1}} \tag{1}$$

Since $V_{BE} \approx v_d$ and r_{ce1} is very large compared with $1/g_m$, equation (1) can be reduced to

$$g_{Tdm} \approx \frac{2i_{C1}}{v_d} = 2g_m \approx \frac{2}{r_e} \approx \frac{2I_{CQ}}{V_T} \tag{2}$$

where g_{Tdm} is the transconductance of the differential-mode operation, g_m is the transconductance of one particular transistor at a time in the input class-AB complementary-pair, I_{CQ} is the dc bias current, and V_T is the thermal-voltage. Thus the differential-mode gain, A_{dm}, of the CFOA is approximately

$$A_{dm} = \frac{2i_{C1}Z_Z}{v_d} = g_{Tdm}Z_Z, \tag{3}$$

where Z_Z is the high impedance of the gain-node of the CFOA.

3. Analysis of common-mode operation

The input stage of the CFOA is the main factor in determining the CMRR performance of the CFOA [9], and [13]. A further study has been made to investigate the parameter that has a direct responsibility towards the common-mode operation, in order to fully understand the inner working of the CFOA, when a common-mode signal is applied to its input. It has been reported that the drawback of the CMRR performance of the CFOA is due to the output impedances of transistors in the input stage [13], [14], and [15]. The currents i_1 and i_2 which flow through the output impedance of Q_1 and Q_2, respectively, as a direct result of the common-mode input voltage V_{cm}, are given by

$$i_1 = \frac{V_{cm}}{r_{ce1}} \text{ and } i_2 = \frac{V_{cm}}{r_{ce2}}. \tag{4}$$

These currents are then mirrored to a high impedance gain-node (Z), where they add algebraically. Thus a high common-mode voltage gain is generated, and a low value of the CMRR is produced, normally in the region of 50dB.

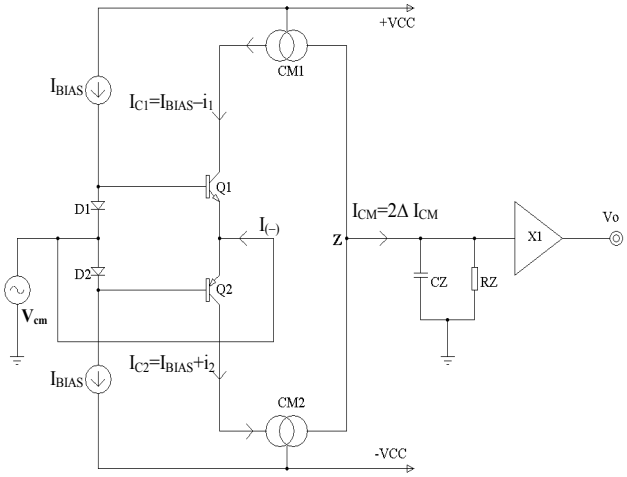

Fig. 3. Circuit schematic of the CFOA with a common-mode input signal, V_{cm}.

Fig. 3 shows a circuit schematic of the CFOA with a common-mode input signal. Applying a positive common-mode input signal decreases the value of V_{CB} of Q_1, and as the Early voltage of this transistor is finite it results in a decrease in the collector current I_{C1} of Q_1 by an amount ΔI_{CM}. Furthermore, the positive common-mode input voltage will cause the value of V_{CB} of Q_2 to rise and, thus, the collector current I_{C2} of Q_2 to increase by the same amount [13], and [15].

Hence, when the collector currents of Q_1 and Q_2 are mirrored by CM1 and CM2 to a high impedance gain-node (Z), the net current into the Z-node is

$$I_Z \approx I_{C2} - I_{C1} = (\Delta I_{CM}) - (-\Delta I_{CM}) = 2\Delta I_{CM} \tag{5}$$

Since $I_{C1} \approx I_{E1}$ and $I_{C1} \approx I_{E1}$, then $I_{(-)} = I_{C2} - I_{C1}$, where $I_{(-)}$ is the inverting node input current. Thus,

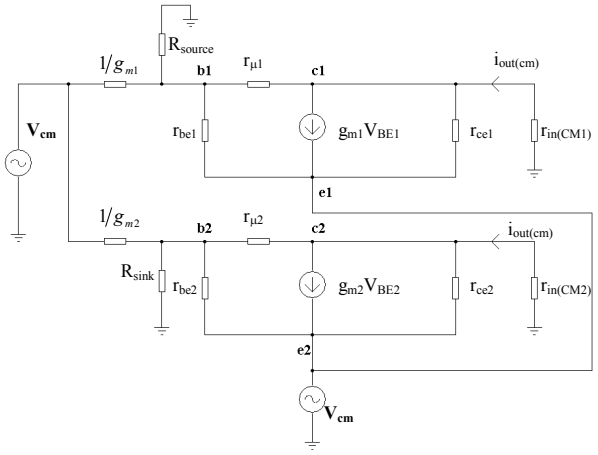

Fig. 4. Small-signal equivalent circuit of the CFOA input stage for common-mode analysis.

$$I_Z \approx I_{(-)} \approx I_{C2} - I_{C1} = 2\Delta I_{CM}\,. \tag{6}$$

To obtain a better understanding, the class AB bias voltage follower (shown in Fig. 3) was analysed using small-signal modelling.

Fig. 4 shows the small-signal equivalent circuit for the input stage of the CFOA driven by an input common-mode voltage signal. Since $1/g_m$, $r_{in(CM1)}$ and $r_{in(CM2)}$ are small, and the bases of Q_1 and Q_2 are connected together, there will be negligible signal voltage across the base to emitter terminals of these two input transistors in Fig. 4 when a common-mode input voltage is applied to the circuit. Hence, both $g_{m1}V_{BE1}$ and $g_{m2}V_{BE2}$ signal current generators are virtually inactive. The net result is that the circuit in Fig. 4 simplifies to the one shown in Fig. 5, and the output current from the coupled current-mirrors, $i_{out(cm)}$, is given by

$$i_{out(cm)} = -2V_{cm}\left[\frac{I_Q}{V_{AN}} + \frac{1}{r_{\mu 1}} + \frac{I_Q}{V_{AP}} + \frac{1}{r_{\mu 2}}\right] \approx -2V_{cm}\left[\frac{I_Q}{V_{AN}} + \frac{I_Q}{V_{AP}}\right], \tag{7}$$

where V_{AN} and V_{AP} are the Early voltages for Q_1 and Q_2, respectively.

Since $r_{\mu 1} \approx r_{\mu 2} >> r_{ce1} \approx r_{ce2} = r_{ce}$, the common-mode transconductance, g_{Tcm}, is given by

$$g_{Tcm} \approx \frac{i_{out(cm)}}{V_{cm}} = -2\left[\frac{I_Q}{V_{AN}} + \frac{I_Q}{V_{AP}}\right]. \tag{8}$$

Thus, the values r_{ce} of Q_1 and Q_2 directly determine the common mode gain, A_{cm}. From equation (8), (A_{cm}=$Vout$/V_{cm}) of the CFOA can be written as

$$A_{cm} = g_{Tcm}Z_Z = \frac{i_{out(cm)}Z_Z}{V_{cm}}\,. \tag{9}$$

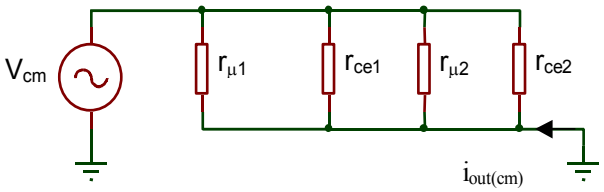

Fig. 5. Reduced small-signal equivalent circuit for the Class AB Bias Voltage Follower.

4. Common-Mode Rejection Ratio (CMRR)

The common-mode rejection ratio (CMRR) is defined as the ratio of the magnitude of the differential gain to the magnitude of the common mode gain [16], and it can be expressed as:

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| \tag{10}$$

where A_{dm} and A_{cm} are the differential mode gain and the common mode gain, respectively. Therefore, by substituting equations (3) and (9) into equation (10) we obtain

$$CMRR = \left|\frac{\dfrac{i_{out(dm)}Z_Z}{V_d}}{\dfrac{i_{out(cm)}Z_Z}{V_{cm}}}\right| = \left|\frac{\dfrac{i_{out(dm)}}{V_d}}{\dfrac{i_{out(cm)}}{V_{cm}}}\right| = \left|\frac{g_{Tdm}}{g_{Tcm}}\right|. \tag{11}$$

Note that the expression of CMRR in equation (11) is independent of the high impedance gain-node Z_Z. Thus, having a higher, or lower, impedance gain-node Z_Z does not influence the CMRR. Now by substituting the expressions of the transconductance of the differential-mode operation of the CFOA, g_{Tdm}, given in equation (2), and of the transconductance of the common-mode operation of the CFOA, g_{Tcm}, given in equation (8), into equation (11) we obtain

$$CMRR = \left|\frac{g_{Tdm}}{g_{Tcm}}\right| = \left|\frac{2I_Q}{V_T}\,\frac{1}{2\left[\dfrac{I_Q}{V_{AN}} + \dfrac{I_Q}{V_{AP}}\right]}\right| = \left|\frac{I_Q}{V_T\left[\dfrac{I_Q}{V_{AN}} + \dfrac{I_Q}{V_{AP}}\right]}\right|. \tag{12}$$

In the special case where $V_{AN} = V_{AP} = V_A$, the expression of CMRR given in equation (12) becomes

$$CMRR = \left|\frac{V_A}{2V_T}\right| \tag{13}$$

Table 1 Variations of CMRR, A_{dm} and A_{cm} with changing values of r_{ce1}, r_{ce2}, r_{e1} and r_{e2}.

Increase parameter	CMRR	A_{dm}	A_{cm}
r_{ce1}, and r_{ce2}	Increases	No change	Decreases
r_{e1}, and r_{e2}	Decreases	Decreases	No change

Table 1 shows the variations of CMRR, A_{dm} and A_{cm} with changing values of r_{ce1}, r_{ce2}, r_{e1} and r_{e2}. To test this theoretical result the full transistor level CFOA shown in Fig. 6 was simulated using SPICE.

This was undertaken using Analog Devices XFCB device parameters. The variations of CMRR, A_{dm} and A_{cm} with changing values of r_{ce1}, r_{ce2}, r_{e1} and r_{e2} are listed in Table 1. The obtained frequency responses of A_{dm}, A_{cm} and CMRR are shown in Fig. 7. The values of the Early voltages V_{AP} of the PNP devices Q_7 and Q_4, and V_{AN} of the NPN device Q_5 and Q_3 were then doubled and the simulation repeated.

These results are shown in Fig. 8. The results presented in Fig. 9 correspond to Early voltages of the input transistors four times greater than the actual AD-XFCB parameters. Although changing the values of V_A in practice is virtually impossible, as a simulation exercise since $r_{ce} \approx V_A / I_{CQ}$, comparison of the results does confirm the anticipated significance of r_{ce} in determining the CMRR of the CFOA.

Comparing the results in Figs. 7 and 8, the values of A_{cm} decreased as expected by 6dB, the values of A_{dm} remained almost unchanged and the CMRR increased by 6dB for each step in doubling of V_A.

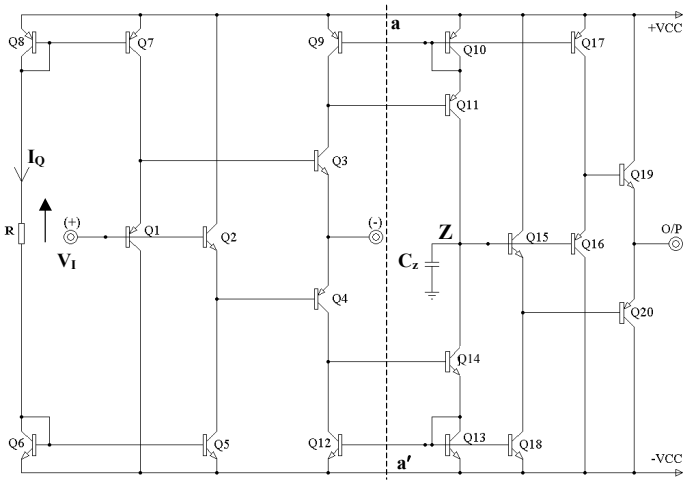

Fig. 6. Full transistor level CFOA.

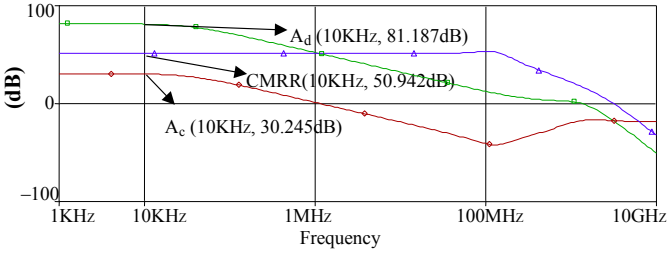

Fig. 7. SPICE results for A_{dm}, A_{cm} and CMRR versus frequency for Fig. 6 using AD-XCFB process parameters.

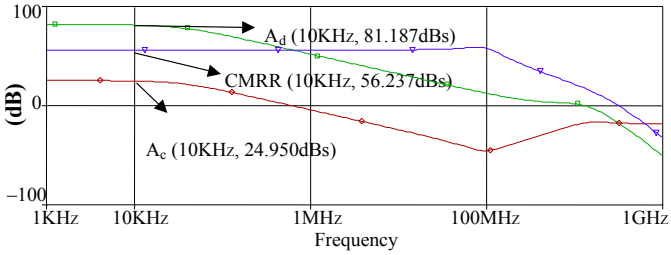

Fig. 8. A_{dm}, A_{cm} and CMRR versus frequency, as in Fig. 7, except that V_A has been doubled for the input stage devices.

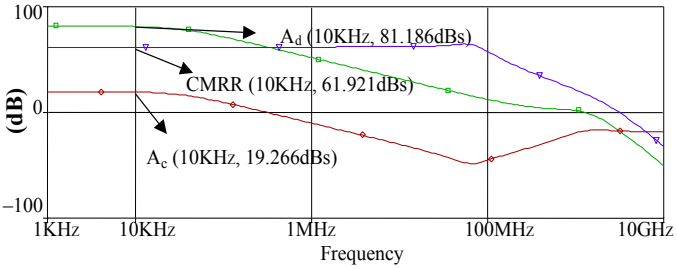

Fig. 9. A_{dm}, A_{cm} and CMRR versus frequency, as in Fig. 8 except that V_A has been quadrupled for the input stage devices.

5. New current feedback operational amplifier

A new CFOA topology is presented in Fig. 10. In theory, the input stage of the CFOA provides an unlimited slew-rate capability. However, in practice the current available to drive the Z-node will always be limited by the biasing currents capabilities in the circuit [17]. But there is trade off relationship between the slew- rate, and the CMRR in the case of the voltage followers, and CFOA [18]. Decreasing the biasing current which is fed to the CFOA circuit seems appropriate since it will minimize the common–mode current flowing through the transistors output resistance of the entire input stage of the CFOA, and hence the common mode will be reduced, which will result in a higher CMRR. Therefore the idea of deploying two biasing currents sources into the CFOA was a step in the right direction of retaining a high bandwidth, and simultaneously increasing CMRR. In addition, to introduce the current-transfer cell that was implemented to cascode the entire input stage, which bleeds for increasing the output impedances of the entire input stage of the CFOA.

Moreover the idea of the new CFOA design is to obtain a good dynamic output range. Transistors Q_{19}/Q_{20} are to give a good slew-rate, while the bootstrapping transistors Q_9/Q_{10} are to

maintain a good CMRR. As for the DC voltage offset each pair transistors Q_1/Q_3, Q_2/Q_4 operate at the same V_{CB}. $(V_2-V_1)\approx 0$, and virtually the same bias currents so that the DC voltage offset is predicted to be very small.

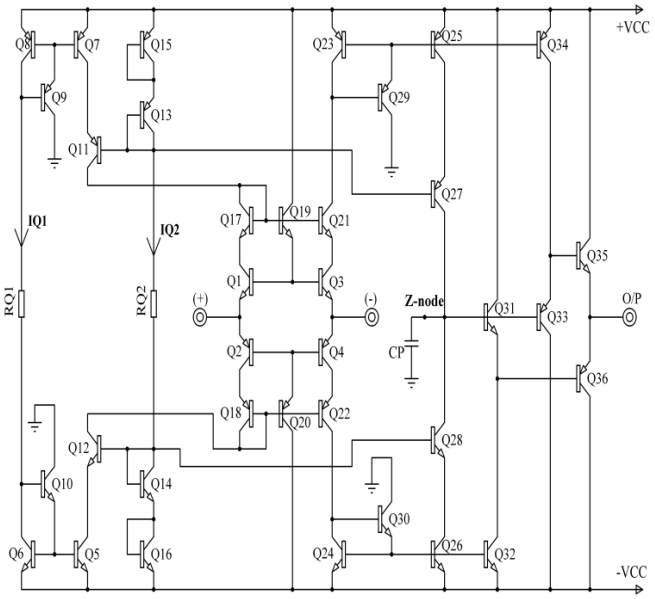

Fig. 10. New CFOA.

6. Modified CFOA

Redesigning the input core a significant improvement will be obtained. This modified circuit of Fig. 10 is shown above in Fig. 11. In this new design the CMRR performance can be further improved, dramatically, by adopting common–mode bootstrapping to the complementary pair transistors Q_3/Q_4. Adding Q_{21}/Q_{23} as well as Q_{22}/Q_{24}, in association with diode-connected transistors $Q_{25}/Q_{26}/Q_{27}$ and $Q_{28}/Q_{29}/Q_{30}$, bootstraps, Q_3/Q_4 by keeping their collector- base voltages virtually constant [19].

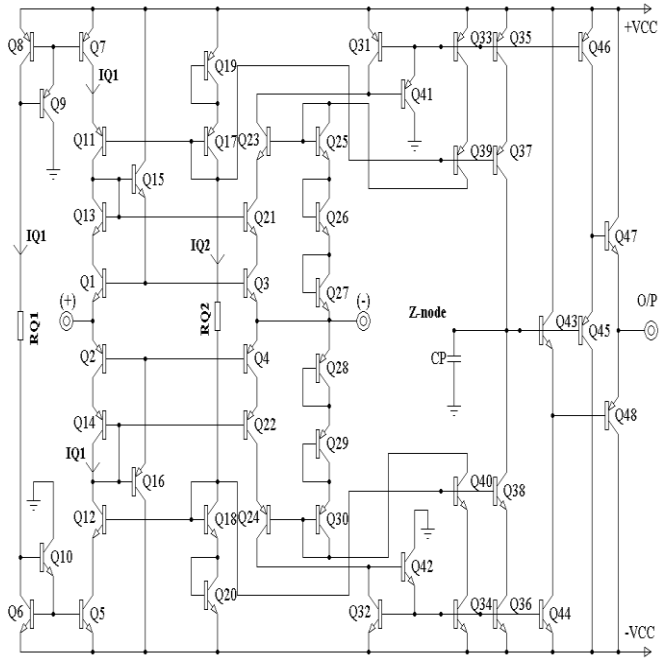

Fig. 11 the modified CFOA of Fig. 10.

7. Simulation Results

SPICE was used to verify the operation and performance of the circuit of Fig 10, and Fig. 11. The technology used in the simulation was the complementary bipolar XFCB process from Analog Devices, Santa Clara. The power supply voltages were set to ±3.8V. For comparative assessment three CFOAs were simulated, namely (i) a conventional CFOA shown in Fig. 6, (ii) the new CFOA deploying two current sources shown in Fig. 10 and (iii) the modified CFOA shown in Fig. 11.

All three CFOA designs were simulated with the same technology parameters, and were set to operate at a bias current equal to 0.14mA. The CMRR simulated results for the conventional CFOA, the modified CFOA and the new CFOA are shown in Fig. 12. Moreover, their individual characteristics are summarized in Table 2. Note that the CMRR is increased to 93.5dB for the modified CFOA and to 90.5dB for the new CFOA while the CMRR for the conventional CFOA remains 50.4dB. Furthermore, the AC gain accuracy has been enhanced for both new CFOAs. Fig. 13 shows the comparisons the graphs of the AC versus frequency for the three CFOAs. With the significant improvements of the bandwidth (see Fig. 17) and CMRR, the modified CFOA shown in Fig. 11 has a superior performance over both the new CFOA deploying two current sources. Moreover, the input referred offset voltage has been reduced for both new CFOAs compared with the conventional design. However, the slew-rate of the conventional amplifier is better than the other two as shown in Fig. 14 as a trade-off. These results are confirmed in Table 2.

By looking at the simulated non-inverting input impedance in Fig. 15, it is clear that the new CFOA deploying two current sources has the poorest non-input impedance of 3.6MΩ. The next best is the conventional CFOA with a non-inverting input impedance of 4.4MΩ. This is about 2MΩ below the non-inverting input impedance of the modified CFOA which has achieved the best performances out of all with a non-inverting input impedance of 6.4MΩ. Fig. 16 shows the frequency responses of all three CFOAs. The bandwidths of the conventional and the new CFOA deploying two current sources, each configured as a unity closed-loop gain amplifier are almost the same. However, the modified CFOA has the widest bandwidth of all three.

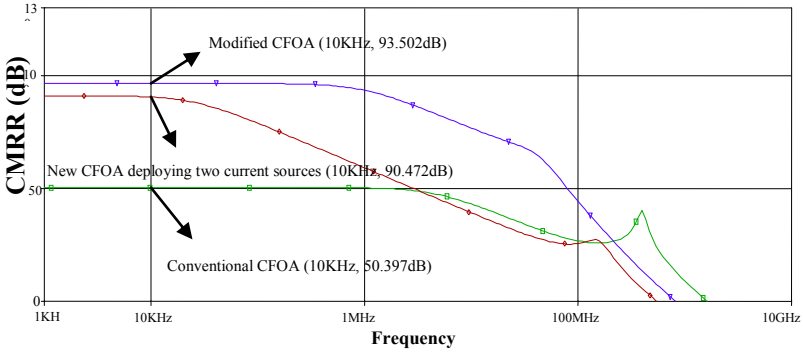

Fig. 12. CMRR~Frequency comparisons

	Conventional CFOA of Fig. 6 [20], [21]	New CFOA deploying two Current Source of Fig. 10	Modified CFOA of Fig. 11
CMRR	50.4dB	90.4dB	93.5dB
Bandwidth	46.8MHz	44.4MHz	120MHz
Non-inverting buffer input resistance	4.4MΩ	3.6MΩ	6.4MΩ
AC gain error (Unity gain, Vin = 1V pp)	3.4mV	100μV	100μV
Input offset voltage	±12.3mV	±1.2mV	±1.4mV
Slew rates	SR+ = 300.2V/μs SR– = 260.9V/μs	SR+ =229.1V/μs SR– =173.5V/μs	SR+ = 274.5V/μs SR– =200.8V/μs

Table 2 Characteristics of the conventional and improved CFOAs for Vcc = ±3.8V

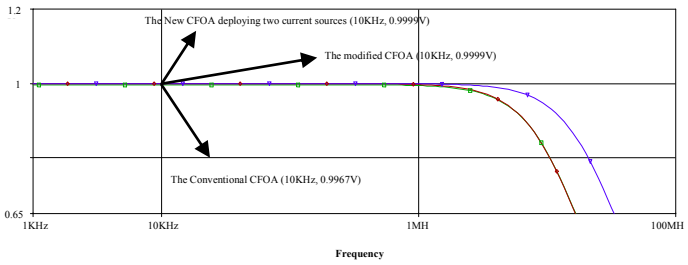

Fig. 13. AC gain accuracy ~ Frequency comparisons.

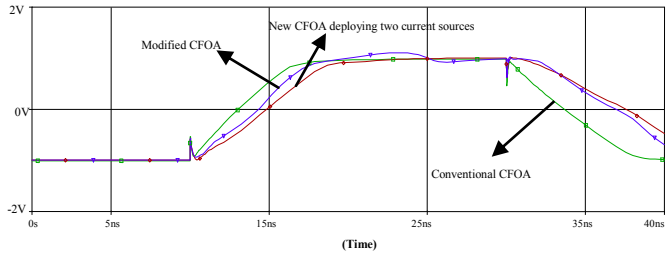

Fig. 14. Voltage ~Time comparisons (The Slew Rate).

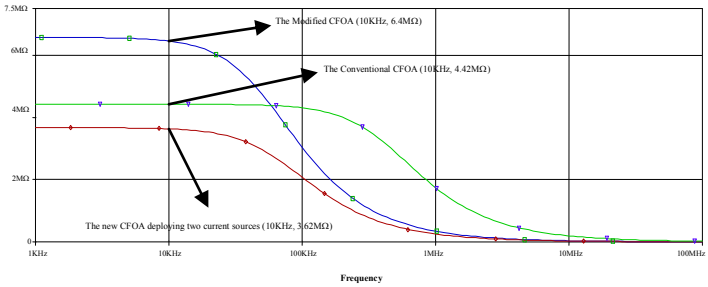

Fig. 15. Input impedance~frequency for the CFOAs, each configured as a non-inverting unity gain amplifier.

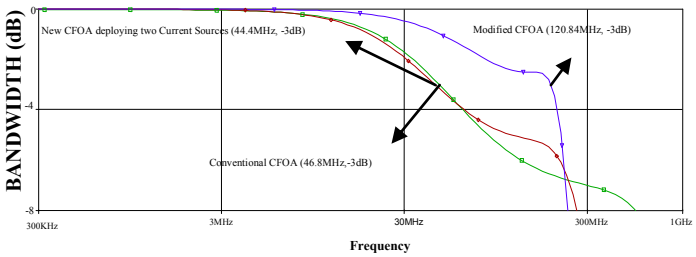

Fig. 16. Bandwidth~ Frequency for unity closed-loop gain comparisons.

9. Conclusion

Two novel CFOA designs have been presented for high accuracy, speed, and CMRR performance. Both new circuits deploy two current sources, one to set the CMRR and the other to set the slew-rate in order to achieve greatly enhanced performance.

The modified CFOA shown in Fig. 11 yields higher non-inverting buffer input resistance with the structure that exhibits an acceptably high slew-rate. In comparison with both CFOAs, the modified CFOA is more efficient. Also other characteristic have been improved, such as higher bandwidth and non-inverting input resistance.

In this paper a MOSFET differential amplifier has been considered because of the growing importance of CMOS in analogue circuit design. However, depending on the application, there may be advantages in implementation in a fully bipolar design. In this case, if Q3, Q4 are the bipolar equivalents of M3, M4, then the presence of Q4 not only partially compensates of the collector-base capacitance of Q3 but it also increases the incremental output resistance seen looking into its collector [7].

The addition of only one transistor, plus bias, into a conventional source-coupled differential amplifer has been shown to extend the CMRR bandwidth substantially. This performance improvement is a result of local feedback reducing the source-coupled node capacitance of the differential pair.

This technique is primarily applicable to an integrated circuit realization of the source coupled differential amplifier because closely matched transistors operating at the same temperature are essential for satisfactory operation. Also the technique can be applied to monolithic instrumentation amplifiers (IAs). Initial results applying the technique to IAs are promising and this work will be the subject of a further publication.

Acknowledgments

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