A Microwatt low voltage bandgap reference for bio-medical applications

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***Abstract*—In this paper a microwatt low voltage bandgap reference suitable for the bio-medical application. The Present technique relies on the principle of generating CTAT and PTAT without using any (Bipolar Junction Transistor) BJT and adding them with a proper scaling factor for minimal temperature sensitive reference voltage. Beta multiplier reference circuit has been explored to generate CTAT and PTAT. Implemented in 45nm CMOS technology and simulated with Spectre. Simulation results shows that the proposed reference circuit exhibits 1.2% variation at nominal 745mV output voltage. The circuit consumes 16uW from 0.8V supply and occupying 0.004875mm2 silicon area.**

Keywords—Opamp, CTAT, PTAT, Beta-multiplier, Bandgap reference, PSRR.

I. INTRODUCTION

Complex Application Specific Integrated Circuits (ASIC) related to the bio-medical field requires temperature stable and power supply independent reference voltage to bias all internal analog circuitry [1][2]. Such a reference should also operate under 1V power supply due to CMOS scaling limitations with minimal output referred thermal noise due to the fact that all biomedical signals are in the uV range. Voltage reference should able to work under noisy environment, due to the noise generated by digital switching

Typical bandgap voltage references [2][3] realized with vertical p-n-p BJTs will have output voltage ~1.2V which are not suitable for less than 1V technologies. Sub 1V reference voltage has been generated by adding shunt resistors across BJT's[4]. In any CMOS technology, vertical BJT's are having poor current gain (β) and large current gain spread, which could contribute significant temperature drift and effects the bandgap voltage accuracy. To mitigate problems with BJT, researchers explored bandgap references with only MOS transistors [5][6]. Mosfet only reference [5] depends on the sub-threshold region which exhibits similar temperature dependency as the BJT. However, most subthreshold voltage references only operate reliably over a limited temperature range. This is because the junction leakage current may severely affect the said subthreshold characteristics. As a result, higher power dissipation is required to achieve wide temperature operation and low-temperature coefficient (TC). [6] has been designed based on body effect of the MOS, which is having severe reliability problem due to forward bias problem and due to body bias substrate noise could enter into the circuit and impacts the circuit sensitivity. The circuit in [7] relies on –ve temperature coefficient of Vth (or gate-source voltage biased with a constant drain current) and which can be used for generating the CTAT voltage and thereby serving the purpose of the BJTs. But the curves of V_{TH} with temperature for any MOS transistor, for different process corners (typical, slow and fast) never converge to a unique point. This is unlike the behaviour of BJTs, where fortunately, all the curves of V_{EB} with temperature for different process corners converge at a unique and precise voltage at 0 K—the bandgap of silicon. Since there is no concept of such a unique voltage for the all CMOS voltage references, such circuits are bound to have significantly larger process variations. The circuit in [8] works on the temperature dependence of NMOS and PMOS threshold voltages. Since V_{THN} and V_{THP} exhibit different CTAT slopes with temperature, they could be in principle, appropriately weighted to create a voltage reference which is constant with temperature. This circuit also suffers from larger untrimmed variations for different process corners as compared to BJT based references. [9] uses zero temperature coefficient of transistor current to develop reference voltage but it results in a complicated circuit hence higher power and thermal noise. The circuit in [10] achieves reference voltage equals to MOS threshold voltage extrapolated to zero absolute temperature to get extreme low voltage operation, but this technique suffers from temperature drift since circuit follows transistor threshold.

The wish list of a voltage reference is sub 1V output voltage, less supply sensitivity, BJT less design, minimal process variation, low noise and less power. For biomedical applications low power and low noise are the major properties. In this paper, a modified beta multiplier circuit has been proposed to fulfill all the requirements explained above. Rest of the paper is organized as follows. Section-II describes interesting properties about existing beta multiplier Quantitatively. Section III describes proposed reference circuit and design constraints for optimal performance. Section IV describes simulation results and circuit layout.

II. REVIEW OF BETA MULTIPLIER REFERENCE.

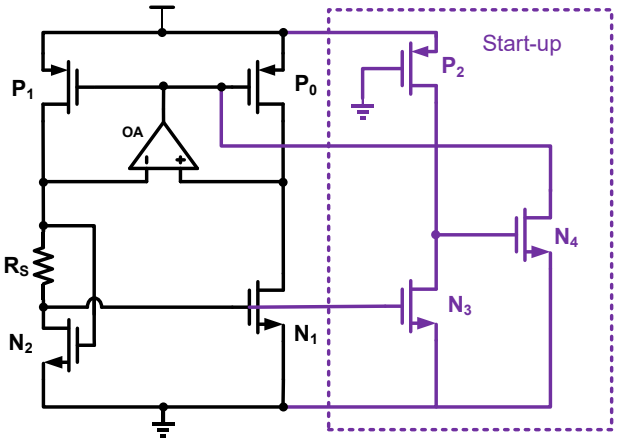

Fig. 1. CMOS Beta multiplier

Fig.1 depicts modified beta-multiplier described in [12]. The Only difference between these two circuits is resistor R_S has been moved from source of N1 to drain of N2 to mitigate body effect. Beta multiplier works as follows. Transistor N_1 is k times larger N_2 such that V_{gs} of N_1 is $\frac{1}{\sqrt{K}}$ times smaller than VGS of N2. The difference of the VGS_{N1} and VGS_{N0} will create current through R_S. Opamp OA senses the drain voltages of N_0 and N_1 and adjusts current through transistors by changing the V_{GS} of pmos transistors. Opamp also reduces the current mismatch between P0 and P1 transistors and increases the loop gain by equalizing Vds. The beta multiplier is dual feedback network. Negative feedback through opamp,P0,N1 and positive feedback through opamp, p1,N2,Rs. For stable operation of any feedback loop positive gain should be less than –ve feedback loop gain to avoid latch-up condition.

Where gmn2 and gmn1 are the trans conductance's of transistors N1,N2. The relation between gmn1,gmn2 are given by $gmn_1 = \sqrt{K}.gmn_2$ (2)

For stable reference, always +ve feedback loop gain should dominate +ve feedback loop gain. Overall loop gain can be derived as

$$Loopgain = \frac{1}{2 - \sqrt{\frac{1}{K}}} \quad (3)$$

From equation (3), we can conclude as long as K greater than 1, the reference loop will be stable. In the present design, it has been chosen as 4. By applying KVL around N1, N2, Rs loop

$VGS_{n2} = VGS_{n1} + IR_s$ and by substituting square law of MOSFET current

$$V_{th} + \sqrt{\frac{2I}{U_n C_{ox}\frac{W}{L}}} = V_{th} + \sqrt{\frac{2I}{KU_n C_{ox}\frac{W}{L}}} + IR_S \quad (4)$$

By solving equation (4) we can deduce Current through N1 as follows.

$$I_{N1} = \frac{2}{U_n C_{ox}\left(\frac{W}{L}\right)} \frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (5)$$

By substituting equation (5) into Trans-conductance equation we can relate $gm_{n2} = \frac{1}{R_S}$ (6)

From Equation (5) it is clearly evident that beta multiplier current is having proportional to temperature (PTAT) nature because the mobility of the electron decreases with temperature. Intuitively voltage across the resistor is the difference of two gate to source voltages, which is PTAT nature hence current through Rs is PTAT. Moreover, the reference current is independent of voltage and threshold voltage (Vth) and only depends on device parameters like transistor size ($\frac{W}{L}$), oxide thickness (t_{ox}) and electron mobility (μ_n). Like any self-bias circuit, beta multiplier also needs to have a startup circuit to make zero current, zero voltage is non stable operating point. Startup circuit consists of N_3,N_4,P_2. When circuit stuck at zero current, the gate voltage of N_3 is stuck at zero hence N_3 drain will stay at vdd such that N_4 draws current from opamp output and pulls down the P_0 gate to below vdd which will then settle at the desired operating point. The size of P_2 and N_3 designed to make sure Drain of N_3 will be close to ground potential in the normal operation. Grounded P2 behaves as a resistor here.

III. PROPOSED BANDGAP REFERENCE.

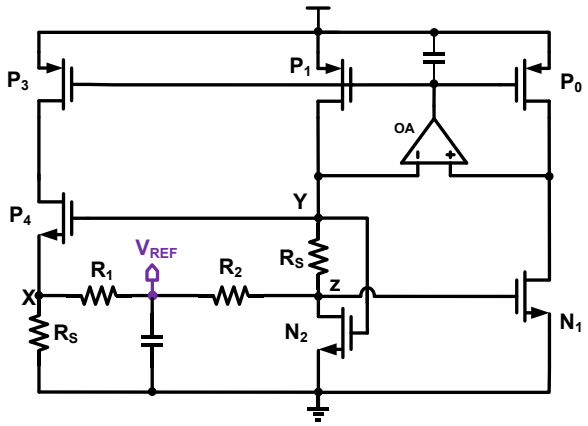

Fig. 2. Proposed bangap reference circuit

Like any bandgap reference, the core principle of the circuit is the addition of scaled version of CTAT and PTAT gives zero temperature sensitive reference voltage. Fig. 2 depicts the proposed reference circuit. N_1,N_2,P_0,P_1 forms beta multiplier for PTAT current generation. P_3,P_4,R_s,R_1,R_2 forms bandgap reference core. Transistor P3 mirrors current from beta multiplier into source degenerated transistor P_4. Transistor P4 has been biased with same V_{gs} as N_2 and P_4 has been degenerated by the same resistance as N_2. The voltage at node X is having PTAT nature because of its current which has been generated by beta multiplier current, this serves as the PTAT voltage for the bandgap. In the beta multiplier, Transistor N_1 gate node Z is heavily depending on V_{th}, and threshold voltage decreases with temperature. By choosing higher value of K (ratio of sizes between N_2 and N_1) Node Z (gate voltage of N_1) voltage can be adjusted as CTAT.

$$I_{N2}=\frac{2}{U_nC_{ox}\left(\frac{W}{L}\right)}\frac{1}{R_S^2}\left(1-\frac{1}{\sqrt{K}}\right)^2 \quad (7)$$

$$V_X=R_S\frac{2}{U_nC_{ox}\left(\frac{W}{L}\right)}\frac{1}{R_S^2}\left(1-\frac{1}{\sqrt{K}}\right)^2 \quad (8)$$

$$=V_{th}+\frac{IR_S}{2\left(1-\frac{1}{\sqrt{K}}\right)} \quad (9)$$

Node z voltage given by

$$V_z=V_{th}+\sqrt{\frac{2I_{N2}}{u_nC_{ox}\frac{W}{L}}} \quad (10)$$

To cancel the temperature coefficient of the reference voltage, CTAT and PTAT has to add with a proper scaling factor, to do this a potential divider R1,R2 has been connected between node X,Z. These resistor values have to be much higher than Rs to reduce the effect of loading.

$$V_{ref}=\frac{V_xR_2+V_yR_1}{R_1+R_2}$$

$$=\frac{1}{1+\beta}\left(V_{th}+\frac{\alpha}{u_nC_{ox}\frac{W}{L}}\right) \quad (11)$$

Where,

$$\alpha=\frac{1}{R_S}\left(1-\frac{1}{\sqrt{K}}\right)\left(\frac{1}{2}+\beta\left(1-\frac{1}{\sqrt{K}}\right)\right)$$

Equation (11) shows how the bandgap reference voltage depends on various parameters of the MOS transistor. Intuitively when temperature increases, first term (Vth) decreases but 2nd term increases because the mobility of an electron decreases with temperature.

IV. OPAMP USED IN THE BANDGAP REFERENCE.

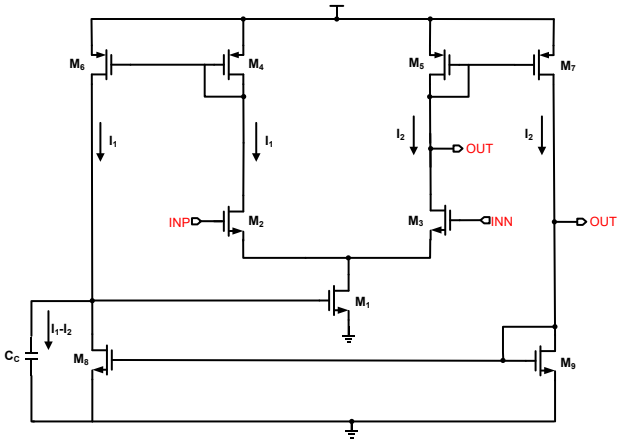

Fig. 3. Opamp used in the reference circuit.

Fig. 3 shows the self-bias opamp used in the bandgap reference circuit [11]. Closed-form expression (11) for reference voltage has been derived under the assumption of zero opamp offset. With opamp offset, reference voltage will change by a small fraction but like any electronic circuit, opamp offset will drift a lot over the industrial temperature range (-40 to 1250C) due to transistor transconductance drift, which will impair the temperature coefficient of the bandgap voltage. A well-known technique self-bias opamp, with this technique 2 times offset improvement has been achieved with self-bias. makes opamp bias current adjusts itself to counteract any temperature dependency. Transistor M2,M3 forms input differential pair, nmos based differential pair has chosen based on input common mode range available from the bandgap.M4,M5 forms diode connected load which converts differential pair small signal current into the output voltage. To bias the opamp tail current transistor M1, a feedback loop formed by M6,M7,M8,M9. Transistors M6,M7 senses the current from the load transistors and amplified the error current M8,M9 common source amplifier stage. Node X will settle by compensation capacitor CC charged by error current i1-i2. Fig-4 shows the input referred offset of the opamp with self-bias and fixed bias (M1 has been biased using a current mirror

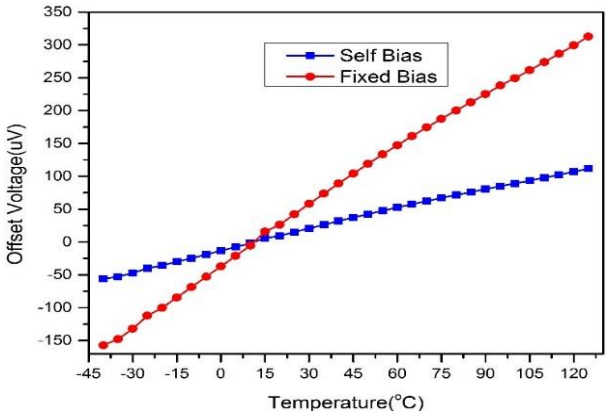

Fig. 4. Simulated Offset of the self-bias Opamp.

V. SIMULATION RESULTS

Proposed bandgap reference circuit is implemented 45nm general purpose CMOS 1poly-8 metal technology. Simulated with post layout extracted circuit with Spectra and results as follows. Designed circuit has been working across wide temperature range and power supply range. Fig. 5 shows temperature sensitivity of the bandgap reference for different process corners (fast, typical, slow). Over the temperature range 2.43mV is the reference voltage variation, hence this design archives 31ppm/^{0}C is the temperature sensitivity while powered from 0.8V supply. The bandgap reference voltage varies only by 2.49mV with power supply variation from 0.6-1.2V, fig. 6 shows the how bandgap voltage varies with power supply. Minimum working power supply 0.6V limitation comes from voltage self-bias opamp input common mode range limitation. Yield play a major role in any electronics circuit, having too much variation across different wafers increases the testing/calibration cost, so as to characterize yield A 6σ Monte Carlo mismatch simulation has been run and fig. 7 shows distribution over 200 runs, from the plot it is clearly evident that standard deviation of the reference voltage is 5.7mV which is ~1.2%. For any reference voltage or current, power supply rejection plays major role when it has been integrated into a big ASIC, since the present voltage reference is based on a –ve feedback loop, up to the loop bandwidth PSRR determined by the loop gain

and beyond bandwidth loop loss control hence it will decrease and mostly depends on transistor output impedance beyond this frequency. Fig. 8 shows the power supply rejection of proposed voltage reference circuit. The power supply rejection ratio (PSRR) is −53.7dB at 100KHz.

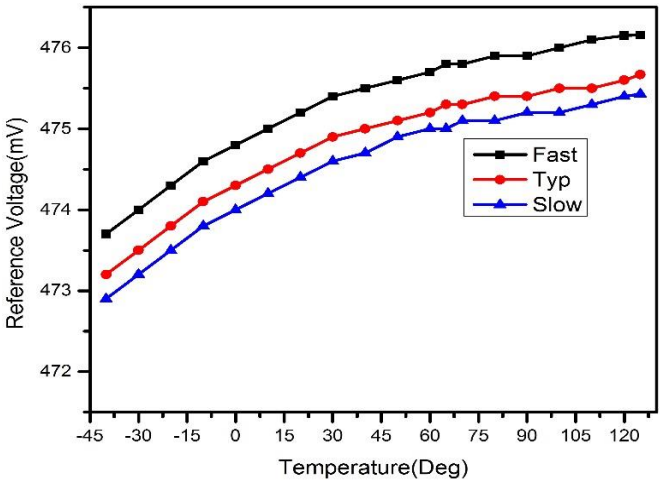

Fig. 5. Simulated Reference voltage with temperature.

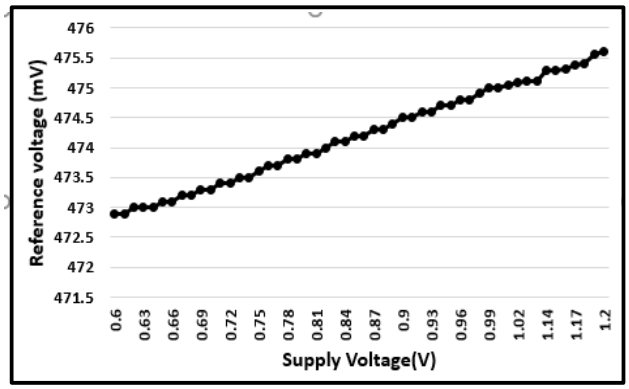

Fig. 6. Simulated Reference voltage with Supply Voltage.

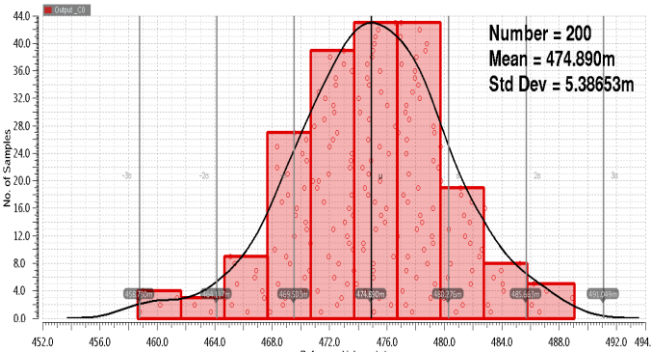

Fig. 7. Monte Carlo variation.

Reference voltage verses Supply Voltage.Fig. 9 shows the output referred noise of the bandgap reference voltage.

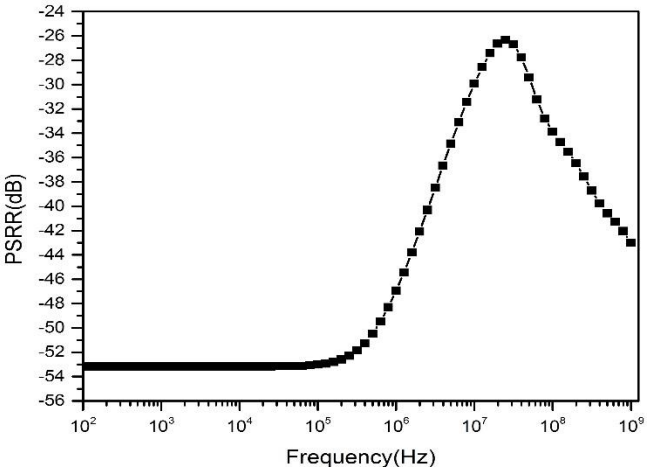

Fig. 8. Simulated Power Supply rejection ratio(PSRR).

Spot noise at 1MHz is -39dB and integrated noise in the band of 10KHz-15MHz is 89uV.The noise achieved is sufficient for all typical applications (VCO bias, touch sensors).

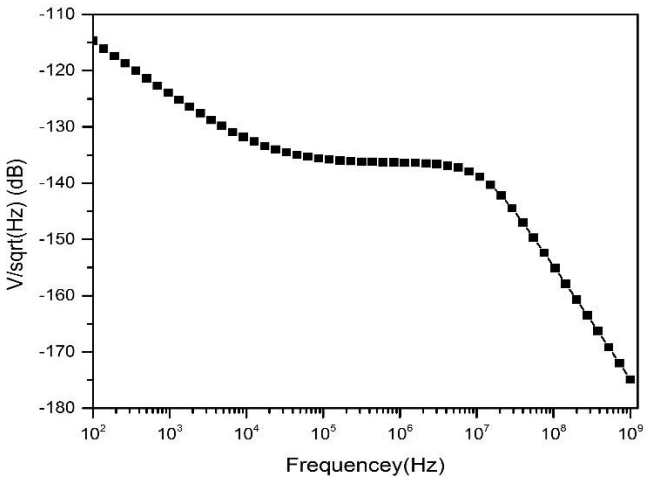

Fig. 9. Simulated output referred Noise.

The layout of the proposed circuit is shown in Fig. 10, and the active area is 81um*64um. Every transistor has been laid with proper care towards Mismatch. Special care has been taken for well proximity effect (WPE) and Shallow trench isolation (STI), by adding enough dummies for each device and keeping MOSFET away from NWELL.

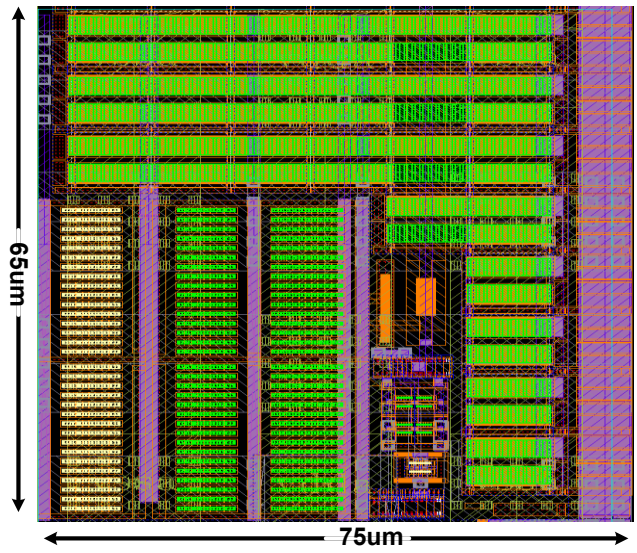

Fig. 10. Layout of bandgap reference..

Table-1 SUMMARIZES the performance of the bandgap circuit.

TABLE-1 PERFORMANCE SUMMARY

Parameter	Result	Unit
Output Voltage	475	mV
Power supply	0.6-1.2	V
Temperature range	-40-125	^{0}C
PSRR @1MHz	-70	dB
Integrated Noise(10KHz-15MHz)	89	uV
Temperature Coefficient	31	ppm/^{0}C
Line Sensitivity	26.5	ppm/V
Power Consumption	16	uW
Technology	45	nm
Area	0.004875	mm^2

VI. CONCLUSION

In this paper, a compact microwatt CMOS bandgap reference utilizing only MOS transistors, which is suitable for wearable biomedical applications. Post layout simulations shows 1.2% variation for a nominal 475mV reference output voltage. Circuit occupies 0.004875 mm^2 silicon area. Implemented in 45nm CMOS and circuit works on 0.8V power supply while consuming 16uW standby power.

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