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Design, Analysis and Experimental Verification of the Self-Resonant Inverter for Induction Heating Crucible Melting Furnace Based on IGBTs Connected in Parallel

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Abstract: The object of this research was a self-resonated inverter, based on paralleled Insulated-Gate Bipolar Transistors (IGBTs), for high-frequency induction heating equipment, operating in a wide range of output powers, applicable for research and industrial purposes. For the nominal installed capacity for these types of invertors to be improved, the presented inverter with a modified circuit comprising IGBT transistors connected in parallel was explored. The suggested topology required several engineering problems to be solved: minimisation of the current mismatch amongst the paralleled transistors; a precise analysis of the dynamic and static transistors' parameters; determination of the derating and mismatch factors necessary for a reliable design; experimental verification confirming the applicability of the suggested topology in the investigated inverter. This paper presents the design and analysis of IGBT transistors based on datasheet parameters and mathematical apparatus application. The expected current mismatch and the necessary derating factor, based on the expected mismatch in transistor parameters in a production lot, were determined. The suggested design was experimentally tested and investigated using a self-resonant inverter model in a melting crucible induction laboratory furnace.

Keywords: induction heating; self-resonant inverter; IGBTs; IGBTs in parallel

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1. Introduction

This paper aimed to design, analyse, prototype, and experimentally test a self-resonant inverter for crucible inductance furnaces to verify the suggested circuit based on IGBTs connected in parallel. For this purpose, a methodology for analysing the transistors' characteristics and the expected mismatch in a production lot was suggested and implied as part of the design procedure. It was based on trend analysis of the transistors' datasheets, digitalising the graphical data and deriving precise polynomial equations. Such a study aimed to compensate for the lack of data on the mismatch of IGBT parameters. In this sense, the presented research's novelty consisted of modifying a well-known circuit, which was analysed with a novel methodology focused on paralleled transistors, giving the expected current mismatch and the necessary derating factor.

As a highly efficient and fast method, induction heating is applicable for numerous technological processes of heating, melting, hardening, etc. The investigated crucible furnaces are used for metal melting, such as gold, steel and copper, applied in different industries—jewellery, steel production, etc. The theoretical basis of induction systems has been described in multiple well-established literature sources [1–6], giving fundamental knowledge for the system inductor-workpiece.

A popular method for induction heating analysis is modelling and simulation with the Finite Element Method (FEM), which depicts the system's electromagnetic field inductor-workpiece. The system's thermal and electrical parameters can be analysed, as well as

the required parameters of the high-frequency electronic converter to be predicted on the simulation level. Using FEM, in [7,8], an induction heating process with a moving inductor or workpiece was presented. Such systems require considerable power to be transferred for a short time for the necessary temperature to be reached at the required time. For this purpose, significant currents through the inductor, for example, 450–890 A at 36 kHz [8], must be supplied from the induction heating inverter. The optimisation of the inductor-workpiece system gave positive results [9] for the magnetic coupling but did not minimise the current provided, presented in most FEM models in the range of 106–108 A/m^2.

According to the research published in [10], the induction heating process with spray cooling, realised by the presented experimental equipment, can continue for a relatively long time at about 30 min. The required inductor current exceeded 400 A. The provided experiments were used for FEM model calibration. A similar study [11], based on the induction heating and FEM modelling analysis, showed a process established at a relatively low frequency of 3 kHz and 544.5 A current through the inductor. Higher frequencies, up to 20 kHz, can be applied for magnetic and nonmagnetic workpieces [12]. The presented experimental verification in [12] was completed with a low-voltage inductor, rated at 47.1 V, which gave a maximum current of 1063 A. In addition, the used capacitor tank at the resonant tank was rated at 15.41 μF or 55.7 μF, which gave a resonant frequency of between 10 kHz and 20 kHz.

Studies focused on the influence of the workpiece characteristics over the heating process [13–15] have shown that the inductor geometry characteristics have a critical impact on the electromagnetic field shape and must be considered with the specific workpiece. This phenomenon has the potential to influence the inverter characteristics influenced by the inductor length and its inductivity and, hence, the resonance frequency with the necessary capacitance tank, as well as the inverter's output current at a given power, which requires additional study.

Another group of recently published papers [16–18], focusing on the development and application of new materials, showed the induction heating application for materials' laboratory production and further investigation. The technological parameters required variations in broad ranges in output power of 10–200 kW, inductor currents up to thousands of amps, low or high inductor voltages and resonant frequencies up to 300 kHz. The exact requirements can be stated for flat-inductor systems [19] and melting induction furnaces [20]. They clearly show that with respect to the industrial equipment with specific parameters, the laboratory induction heating must be much more flexible, which would ensure its application for different laboratory tests and studies. According to these requirements, self-oscillating inverters for induction heating are good candidates for laboratory equipment as a simple structure that is highly reliability and naturally operating with inherent Zero Voltage Switching (ZVS) modulation, which gives low switching losses. In [21–23], a self-oscillating inverter with a parallel resonant tank operating at a relatively low power of 300 W was proposed. The research showed the advantages of implementing a Current Source Parallel Resonant Push-Pull Inverter (CSPRPI) and the possibilities of achieving ZVS with low switching losses. A similar topology based on a half-bridge but a series resonant tank was also proven to have a stable operation at ZVS [24]. Furthermore, the same source proved that these classes of converters can be controlled with a simple phase-locked loop based on a variable duty cycle.

A converter structure with proven application in induction heating, giving high power density and the ability to operate with soft-switching, is the full-bridge circuit with a parallel or series resonant tank, based on different modulation techniques, such as Phase-Shift Modulation (PSM), Pulse-Frequency Modulation (PFM), Pulse-Density Modulation (PDM) and Asymmetrical Duty-Cycle (ADC) [25–31]. These types of modulation offer flexible control over the wide range of output powers [25]. These inverters applied for induction heating can have a good match with a Power Factor Correction (PFC) stage [26]. An additional characteristic of the PSM is the ability of the ZVS to be achieved for the required

power range under regulation with variable switching frequency [27]. It has been shown that the use of variable switching has a better efficiency than a fixed switching frequency. Despite the modulation technique, the problem with the transient overvoltages and electromagnetic interference (EMI) due to the transistor switching is mitigated with snubbers.

In contrast to the self-oscillating inverters [21–23], one of their advantages is usually based on snubber-less power stage circuits for the full-bridge PSM topology, and different types of passive snubbers such as C, RC, and RCD can be used. Their selection and design depend on the modulation technique and the match between the used IGBTs and the resonant tank parameters [28,29]. In the same class, transformer-based converters are the LLC resonant inverters. A powerful inverter of this type, rated at 25 kW with a fixed frequency of 25 kHz, is presented in [30]. Transformer-less topologies based on a full-bridge can be realised as matrix converters, whose topology requires bi-directional switches [31]. Although these converters have significant advantages, a comparative analysis shows that the self-resonant converters are based on a more straightforward structure, giving a budget-friendly induction heating system, with low EMI, without snubber circuits and low losses.

Another group of papers focused on induction heating devices for cooking [32–36], which usually have flat inductors and an installed power in the range of 1.5–2.8 kW. According to their shapes and materials, an important issue is the magnetic coupling between the inductor and the loads, i.e., pan, pot and wok [32,33]. The other parts of the control system: sensors, feedbacks, filters, etc., are also well investigated from the cooking-intended induction heaters [34–36]. The reported efficiency for cooking induction heating converters is over 95%, which can be expected as a parameter for a powerful induction heating crucible system.

The provided literature review concludes that the self-oscillating resonant converters have the simplest circuit, offering a robust and budget-friendly solution. Currently, they are applied for relatively low power in the range of 300–800 W as laboratory equipment, using cylindrical inductors for heating magnetic elements [37,38]. It can be suggested that their application can be extended to more considerable powers, over 30 kW, and a frequency range of 25–35 kHz, giving an application for fast-melting crucible inductance furnaces [39]. Such a power would require a power stage based on IGBT transistors connected in parallel to be designed and implemented. Numerous papers [40–47] present research mainly focused on IGBTs. Current equalisation with improved gate drive control implemented with Digital Signal Processors (DSPs) and precise current measurements is given in [40,41]. Strategies based on active driver circuits and current cross-reference control techniques were proposed in [42], including for Silicon Carbide (SiC) MOSFETs [43,44].

Nowadays, Revers Conducting IGBTs (RC-IGBTs), specialised for resonant inverters, i.e., applicable for induction heating systems, are offered by manufacturers [45–48]. According to the presented applications [45], the analysis of the transistors' technology and their implementation in the induction inverters [47] justifies the suggestion that paralleled RC-IGBT can operate with a good current sharing and, hence, low current mismatch. The experimental data presented with oscillograms showed inverters' soft-switching operation [45,47–50] in the induction heating resonant inverters. Furthermore, the assembling procedure applied for half-bridge resonant inverters [46] implies that current equalisation for the self-resonant induction converters based on paralleled IGBTs can be easily achievable. All of the stated suggestions require additional analytical and experimental research as such has not been found in the literature. Some statistical information about the parameters' dispersion of IGBT modules is given in [50], but no analysis or experimental data have been found for discrete transistors.

As a conclusion from the presented literature review: the self-resonant converters for induction heating [21–24] are an applicable technology giving reliable and budget-friendly solutions; induction heating inverters, with an installed power higher than 10–15 kW for industrial and laboratory research purposes [29–31], can be constructed by IGBT transistors connected in parallel, but the literature presenting such applications specifically

for self-resonated inverters is insufficient; although the paralleling of transistors is an object of significant research [40–44], the application of this topology in the self-resonance architectures requires additional investigation. In general, from the literature, it is clear that the topology of self-resonant inverters for induction crucible melting furnaces has the potential to reach higher powers with paralleled transistors. However, the undesirable phenomena caused by transistors' parameters mismatches are not well described in the literature specifically for this application. Furthermore, the parallel operation in the resonant inverters can cause problems such as uneven current allocation, operation outside the ZVS region and major malfunction.

Based on the presented literature findings, the primary purpose of the suggested research was to experimentally show the possibility of resonant inverters with paralleled IGBTs operating with improved characteristics. For this purpose, a methodology for the analysis of transistors' characteristics was developed, giving a precise estimation of the paralleling IGBTs abilities. The presented approach estimated the derating factors and the expected current share through digitalising the graphical data and conducting a thorough analysis.

The paper is organised as follows: Section 2 shows an analysis of the modified self-resonated inverter based on the suggested methodology for analysis of the transistors connected in parallel; Section 3 shows an experimental verification; the conclusions are presented in Section 4.

2. Analysis of the Investigated Inverter, Based on RC-IGBTs in Parallel

The self-resonated converter is shown in Figure 1. The object of this research was the power stage of the inverter, which is part of the entire system presented with a block diagram. The further analysis and the experimental model presented in Section 3 were completed with discrete RC-IGBTs. In this circuit, it is necessary for the transistors' emitters to be connected at a common point (GND); off-the-shelf half-bridge IGBT modules would not be suitable. Analysing the IGBTs currently available on the market, the targeted power for the designed crucible melting induction system in a range of 20–30 kW, with a potential to reach 50 kW, could be achieved with 3 to 8 high and low side transistors connected in parallel. Such a circuit applies the necessity of a precise analysis of the IGBTs parameters to be undertaken due to the specific parasitic elements that the discrete packages, usually TO-247, TO263, etc., and their modification typically have. The gate drive circuits are based on optical drivers to supply the necessary gate drive current. An additional obstacle is the lack of information about the expected mismatch of transistors' parameters in a production lot, usually not published by the manufacturers.

The block diagram presented in Figure 1 is arranged as follows: (1) the three-phase rectifier and power factor correction (PFC) module are based on a full-bridge circuit, followed by a Boost PFC converter controlled by an ASIC (Application Special Integrated Circuit); (2) the Buck converter is a transformer-less PWM converter, but for safety purposes, a transformer-based full-bridge converter can be considered; (3) the resonant inverter was the object of this research, depicted in the power circuit. As the circuit is self-resonated, the control module operates as overcurrent and overvoltage protection, with the functionality to shut down the inverter; (4) the feedback from the inductor is performed by isolated current and voltage sensors; (5) the control and protection system is based on an STM microcontroller, including feedback networks from each module.

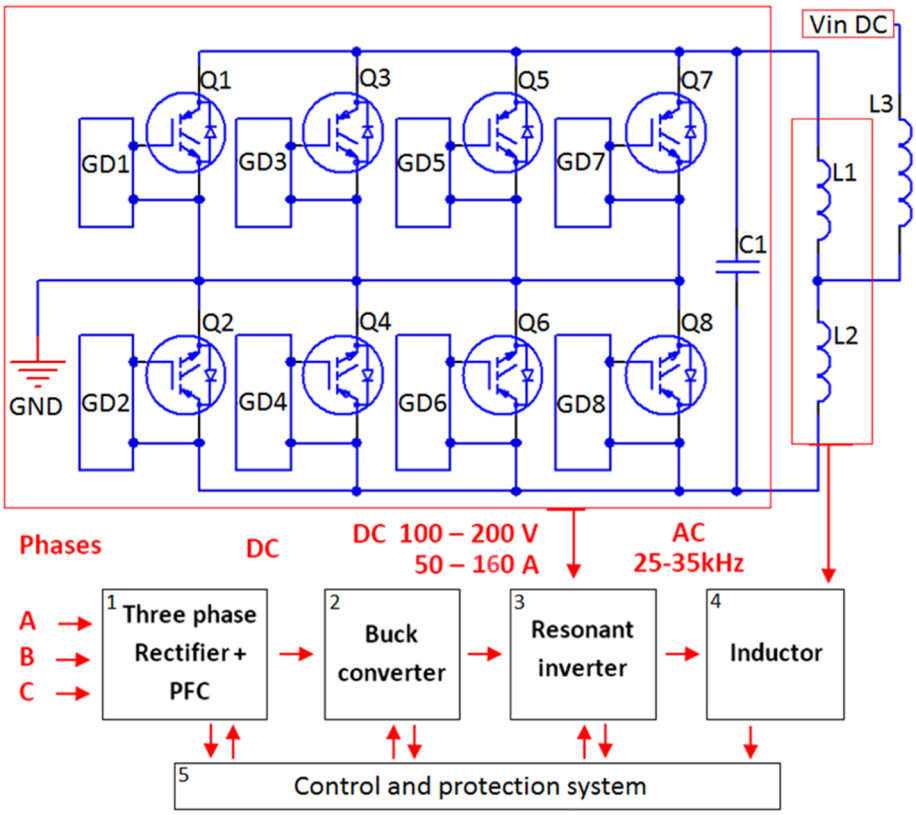


Figure 1. The electronic circuit of the proposed inverter for induction heating crucible melting furnace. Q1-Q8 IGBT transistors; GD1-GD8 gate drivers; C1, L1, L2 resonance tank; L3 induction heating inductor. A block diagram of the entire system for induction heating.

The steady-state and transient conditions caused, respectively, by the saturation collector-emitter voltage $V_{CE(sat)}$ and the variations in the gate-emitter threshold voltage $V_{GE(th)}$ of the IGBTs connected in parallel and, associated with them, thermal dependencies, are the most critical parameters, which must be analysed. The suggested methodology was focused on in the analysis of the variations in the transistors' parameters and the estimation of the probable current mismatch, which was designed in several steps as follows [51–55]:

Step 1. Estimating the necessary derating factor and total current.

Calculation of the derating factor Δ:

$$\Delta = 1 - \frac{I_{max}}{N_{parallel} \times I_{IGBTmax}} \tag{1}$$

where I_{max} is the maximum current through all transistors connected in parallel, $N_{parallel}$ is the number of IGBT transistors in parallel, connected in the high or low side of the circuit given in Figure 1, $I_{IGBTmax}$ is the maximum current per IGBT transistor. The result from this equation under the satisfactory deration requires the number of transistors or $I_{IGBTmax}$ to be increased.

At a given derating factor, the total current in a parallel I_{Total} is:

$$I_{Total} = (1 - \Delta) \times N_{parallel} \times I_{IGBTmax} \tag{2}$$

For the designed and experimentally tested inverter for induction heating, the maximum current of $I_{max} = 160\ A$ is assumed. Equation (1) is calculated for 2 to 6 transistors in parallel, and the derating factor is in the range $\Delta = 0.1 - 0.5$; the result is depicted in Figure 2A. Following the recommendations given by IGBT manufacturers and the industrial research on induction heating [45–47], as a first assumption, a derating factor of

$\Delta = 0.2$ is accepted. A suitable transistor technology for a resonant inverter can be chosen (Trenchstop, Trench gate field-stop, etc., RC-IGBT [48,49]) with Positive Thermal Coefficient (PTC). Considering the current ranges for the discrete IGBT transistors, assembled in TO-247, TO-3PN, TO-264, etc. packages, the feasible current capacity would be 50–160 A, as shown in Figure 1. With this assumption, four transistors are accepted for this design. The analysis shows that the datasheet transistor current must be selected at $I_C = 50$ A (Figure 2A), the expected current through each transistor is 40 A (Figure 2B) calculated from Equation (2), and the specific derating factor is $\Delta = 0.2$ (Figure 2C). Several IGBTs, which have been used for the analysis and experimental verification, are presented in Table A1, Appendix A.

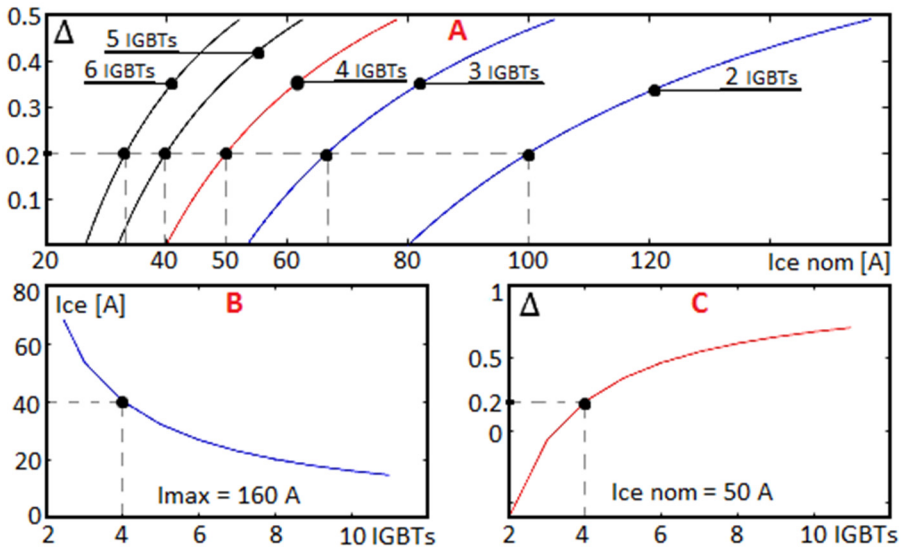


Figure 2. Analysis of the number of IGBTs in parallel. (**A**) Number of transistors in parallel calculated in a derating range $\Delta = 0.1 - 0.5$, giving the necessary nominal current per transistor; (**B**) expected current through each transistor at the assumed maximum current of $I_{max} = 160$ A; (**C**) the targeted derating of $\Delta = 0.2$, i.e., 20%, is feasible with $I_{CEnom} = 50$ A, 4 IGBTs in parallel.

Step 2. Selecting the IGBT, digitalising the necessary datasheet graphics and analysing the obtained data.

The critical parameters for this analysis, given in the datasheets as diagrams, are shown as examples in Figure 3 as the transconductance characteristic (Figure 3A) and the output characteristic (Figure 3B).

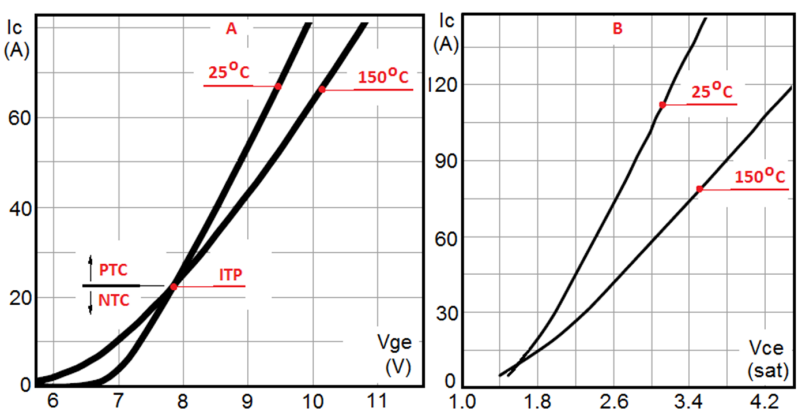


Figure 3. (**A**) IGBT transconductance characteristic and its dependence on the temperature; NTC—Negative Thermal Coefficient; PTC—Positive Thermal Coefficient; ITP—Isothermal Point; (**B**) IGBT output characteristics and its dependence on the temperature.

Using the IGBTs datasheet in the design procedure shows several problems that prevent a precise analysis of the paralleled transistors from being completed:

- The variation in parameters in a production lot is not apparent and cannot be analysed. Hence, the expected current variation amongst the paralleled transistors and the necessary deration factor cannot be precisely estimated.
- The precise position of the Isothermal Point (ITP, Figure 3A) and its variations, which depend on the variations in V_{ge} and I_C, cannot be precisely estimated. This means that the designed converter would not operate under a stable Positive Thermal Coefficient (PTC) at any mode of operation, rather than a Negative Thermal Coefficient (NTC).
- There are expected variations in the Collector-Emitter voltage drop $V_{CE\ (sat)}$. Hence, the expected losses and their distribution amongst the paralleled transistors cannot be precisely estimated in a production lot.

The suggested methodology offers a solution to the stated problems as follows:

- Digitalising the graphical data available from the transistors' datasheets and converting them into equations using trend analysis. Figure 4 shows the digitalising graphics product of solving polynomial equations.
- Deriving the expected parameters variation in a production lot. A variation of ±5% can be accepted, based on the provided manufacturers' statistical [50] and experimental [51,53,54] research. The expected variation in the static characteristics is presented in Figure 4A—graphics 1–2 and graphics 3–4 parameters variations, respectively, at nominal 25 °C and maximum 150 °C temperatures. Following the same sequence, the expected variation in the dynamic characteristics is given in Figure 4B.
- Estimating the expected derating factor and current mismatch based on the expected variation. The result shows the variation in the derating factor and justifies the assumption made from Equations (1) and (2), presented in Figure 2. It also shows the PTC established at the selected V_{ge} in the entire range of the static parameters.

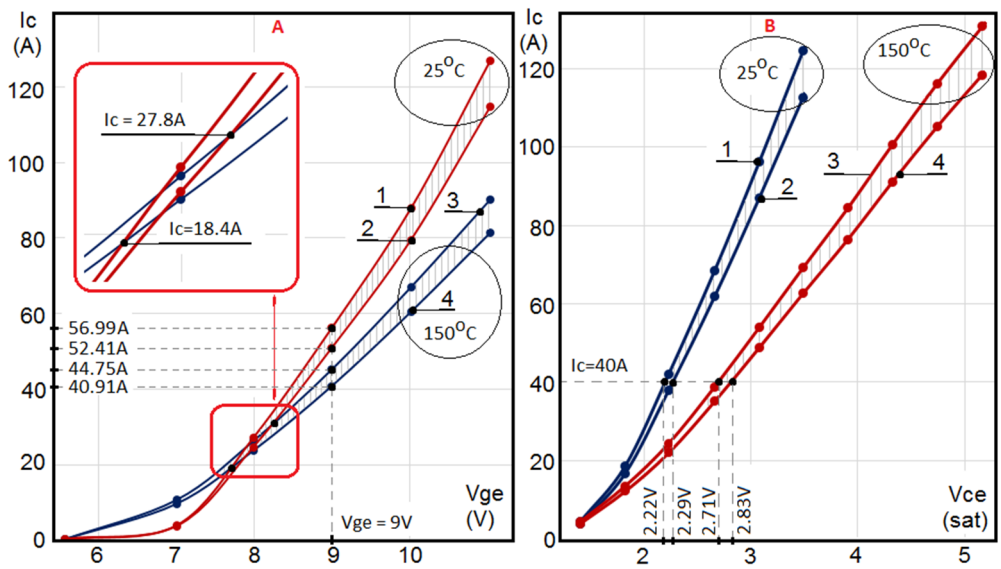


Figure 4. (**A**) Transconductance (dynamic) characteristics at nominal 25 °C (graphic 1 maximum and 2 minimum) and maximum 150 °C (graphic 3 maximum and 4 minimum) temperatures. (**B**) Output (static) characteristics at nominal 25 °C (graphic 1 maximum and 2 minimum) and maximum 150 °C (graphic 3 maximum and 4 minimum) temperatures.

The equations, products of the trend analysis obtained from the IGBTs datasheet (Figure 3), would be a polynomial of 4–6 degrees in order for the parameters to be described with greater precision.

Nominal transconductance characteristic, at nominal temperature 25 °C (Figure 3):

$$I_C = \left(0.0091 \times V_{GE}^5\right) + \left(-0.1009 \times V_{GE}^4\right) + \left(-3.6877 \times V_{GE}^3\right) + \left(82.845 \times V_{GE}^2\right) + (-571.73 \times V_{GE}) + 1300.2 \quad (3)$$

Maximum transconductance characteristic (Figure 4, graphic 1), i.e., +5% from Equation (3):

$$I_C = \left(0.0096 \times V_{GE}^5\right) + \left(-0.106 \times V_{GE}^4\right) + \left(-3.8721 \times V_{GE}^3\right) + \left(86.988 \times V_{GE}^2\right) + (-600.32 \times V_{GE}) + 1365.2 \quad (4)$$

Minimum transconductance characteristic (Figure 4, graphic 2), i.e., −5% from Equation (3):

$$I_C = \left(0.0087 \times V_{GE}^5\right) + \left(-0.0959 \times V_{GE}^4\right) + \left(-3.5033 \times V_{GE}^3\right) + \left(78.703 \times V_{GE}^2\right) + (-543.15 \times V_{GE}) + 1235.2 \quad (5)$$

Nominal transconductance characteristic, at high temperature 150 °C (Figure 3):

$$I_C = \left(-0.0278 \times V_{GE}^5\right) + \left(1.2169 \times V_{GE}^4\right) + \left(-21.274 \times V_{GE}^3\right) + \left(186.96 \times V_{GE}^2\right) + (-812.84 \times V_{GE}) + 1381.6 \quad (6)$$

Maximum transconductance characteristic (Figure 4, graphic 3), i.e., +5% from Equation (6):

$$I_C = \left(-0.0292 \times V_{GE}^5\right) + \left(1.2777 \times V_{GE}^4\right) + \left(-22.338 \times V_{GE}^3\right) + \left(196.31 \times V_{GE}^2\right) + (-853.48 \times V_{GE}) + 1450.6 \quad (7)$$

Maximum transconductance characteristic (Figure 4, graphic 4), i.e., −5% from Equation (6):

$$I_C = \left(-0.0264 \times V_{GE}^5\right) + \left(1.156 \times V_{GE}^4\right) + \left(-20.211 \times V_{GE}^3\right) + \left(177.61 \times V_{GE}^2\right) + (-772.2 \times V_{GE}) + 1312.5 \quad (8)$$

The derived equations are presented as matrices in Table 1. Such a format is suitable for calculation with a simple Matlab script, shown in Listing A1 the Appendix A. The designed converter is depicted in Figure 4 as $V_{ge} = 9$ V, and the expected maximum collector current due to the temperature and parameters variation would be $I_{Cmax(150^\circ\mathrm{C},min)} = 40.91$ A, $I_{Cmax(150^\circ\mathrm{C},\,max)} = 44.75$ A, $I_{Cmax(25^\circ\mathrm{C},min)} = 52.41$ A, and $I_{Cmax(25^\circ\mathrm{C},max)} = 56.99$ A. This analysis shows that the current can vary by 16 A under the worst-case conditions, i.e., if the paralleled transistors operate at the minimum and maximum temperature, assembled on different heatsinks and operating under specific cooling conditions, etc. Although such a thermal condition is less probable to be established, the correct design must consider it. If the paralleled transistors shared the same thermal conditions at the maximum temperature, the maximum current mismatch would be 4.58 A, i.e., under 20% of the maximum current. It can be expected that the accepted $\Delta = 0.2$ would be a correct assumption.

Table 1. Digitalisation of the transconductance characteristics, shown in Figure 4A.

	nominal characteristic (Figure 2)	+5% data variation Figure 3A, graphic 1	−5% data variation Figure 3A, graphic 2
Nominal temperature 25 °C	$I_C = \begin{bmatrix} 0.0091 \times V_{GE}^5 \\ -0.1009 \times V_{GE}^4 \\ -3.6877 \times V_{GE}^3 \\ 82.845 \times V_{GE}^2 \\ -571.73 \times V_{GE} \\ 1300.2 \end{bmatrix}$	$I_C = \begin{bmatrix} 0.0096 \times V_{GE}^5 \\ -0.106 \times V_{GE}^4 \\ -3.8721 \times V_{GE}^3 \\ 86.988 \times V_{GE}^2 \\ -600.32 \times V_{GE} \\ 1365.2 \end{bmatrix}$	$I_C = \begin{bmatrix} 0.0087 \times V_{GE}^5 \\ -0.0959 \times V_{GE}^4 \\ -3.5033 \times V_{GE}^3 \\ 78.703 \times V_{GE}^2 \\ -543.15 \times V_{GE} \\ 1235.2 \end{bmatrix}$
	Nominal characteristic (Figure 2)	+5% data variation Figure 3A, graphic 3	−5% data variation Figure 3A, graphic 4
Maximum temperature 150 °C	$I_C = \begin{bmatrix} -0.0278 \times V_{GE}^5 \\ 1.2169 \times V_{GE}^4 \\ -21.274 \times V_{GE}^3 \\ 186.96 \times V_{GE}^2 \\ -812.84 \times V_{GE} \\ 1381.6 \end{bmatrix}$	$I_C = \begin{bmatrix} -0.0292 \times V_{GE}^5 \\ 1.2777 \times V_{GE}^4 \\ -22.338 \times V_{GE}^3 \\ 196.31 \times V_{GE}^2 \\ -853.48 \times V_{GE} \\ 1450.6 \end{bmatrix}$	$I_C = \begin{bmatrix} -0.0264 \times V_{GE}^5 \\ 1.156 \times V_{GE}^4 \\ -20.211 \times V_{GE}^3 \\ 177.61 \times V_{GE}^2 \\ -772.2 \times V_{GE} \\ 1312.5 \end{bmatrix}$

Following the same data presentation format, the necessary equations for the static transistor's characteristics are given in Table 2. At the calculated points, the selected transistor would operate with PTC, considering the variations in the ITP under the worst-case conditions shown in Figure 4A. The voltage collector-emitter at the nominal expected current through each transistor of $I_C = 40$ A (Figure 4B) is $V_{CE(sat\ 25^\circ\mathrm{C}\ max)} = 2.22$ V, $V_{CE(sat\ 25^\circ\mathrm{C}\ min)} = 2.29$ V, $V_{CE(sat\ 150^\circ\mathrm{C}\ max)} = 2.71$ V, and $V_{CE(sat\ 150^\circ\mathrm{C}\ max)} = 2.83$ V. The result shows that the expected conductive losses, which are the primary losses for the analysed ZVS inverter, are feasible for the TO-273 transistor package and its modifications, as shown in Table A1, Appendix A.

Table 2. Digitalisation of the output characteristics shown in Figure 4B.

	nominal characteristic (Figure 2)	+5% data variation Figure 3B, graphic 1	−5% data variation Figure 3B, graphic 2
Nominal temperature 25 °C	$I_C = \begin{bmatrix} -1.2487 \times V_{CE}^5 \\ 17.285 \times V_{CE}^4 \\ -96.404 \times V_{CE}^3 \\ 274.79 \times V_{CE}^2 \\ -342.33 \times V_{CE} \\ 146.59 \end{bmatrix}$	$I_C = \begin{bmatrix} -1.3112 \times V_{CE}^5 \\ 18.149 \times V_{CE}^4 \\ -101.22 \times V_{CE}^3 \\ 288.53 \times V_{CE}^2 \\ -359.45 \times V_{CE} \\ 153.92 \end{bmatrix}$	$I_C = \begin{bmatrix} -1.1863 \times V_{CE}^5 \\ 16.421 \times V_{CE}^4 \\ -91.583 \times V_{CE}^3 \\ 261.05 \times V_{CE}^2 \\ -325.21 \times V_{CE} \\ 139.26 \end{bmatrix}$
	Nominal characteristic (Figure 2)	+5% data variation Figure 3B, graphic 3	−5% data variation Figure 3B, graphic 4
Maximum temperature 150 °C	$I_C = \begin{bmatrix} -0.0371 \times V_{CE}^5 \\ 0.7896 \times V_{CE}^4 \\ -7.2327 \times V_{CE}^3 \\ 34.392 \times V_{CE}^2 \\ -46.567 \times V_{CE} \\ 18.897 \end{bmatrix}$	$I_C = \begin{bmatrix} -0.039 \times V_{CE}^5 \\ 0.8291 \times V_{CE}^4 \\ -7.5943 \times V_{CE}^3 \\ 36.111 \times V_{CE}^2 \\ -48.895 \times V_{CE} \\ 19.842 \end{bmatrix}$	$I_C = \begin{bmatrix} -0.0353 \times V_{CE}^5 \\ 0.7501 \times V_{CE}^4 \\ -6.8711 \times V_{CE}^3 \\ 32.672 \times V_{CE}^2 \\ -44.238 \times V_{CE} \\ 17.952 \end{bmatrix}$

Step 3. Analysing the mismatch and the derating factor for the stationary and dynamic transistors' characteristics.

The mismatch factor M can be estimated from the maximum and minimum current at the given conditions from the equation:

$$M = \frac{I_{C\ max} - I_{C\ min}}{I_{C\ max}} \tag{9}$$

where $I_{C\ max}$ and $I_{C\ min}$ are the maximum and minimum current per IGBT transistor in parallel, respectively, calculated in Step 2.

Having the mismatch factor M and the accepted IGBTs in parallel, Equation (1) about the derating factor Δ can be presented as:

$$\Delta = 1 - \frac{\left(N_{parallel} - 1\right)(1 - M) + 1}{N_{parallel}} \tag{10}$$

The result from Equations (9) and (10) is depicted in Figure 5. In the range $V_{ge} = 9$–10 V, the derating factor varies in the range $\Delta = 0.12$–0.21 under the worst-case conditions, which would occur at nonthermal equivalence amongst the transistors (Figure 5A, graphic 1). The result shows that the accepted $\Delta = 0.20$ at Step 1, Equation (1), is a correct assumption. If the paralleled transistors share the same thermal equilibrium, the necessary derating factor would be in the range $\Delta = 0.034$–0.053, i.e., 3.4%–5.3%. Under these conditions, the system based on a 20% derating factor, matching the probable worst-case condition, would be oversized under thermal equalisation. This result is supported by an expression of the

current difference in Figure 5B—graphic 1 shows the maximum current difference under the worst-case conditions and graphic 2 at thermal equalisation.

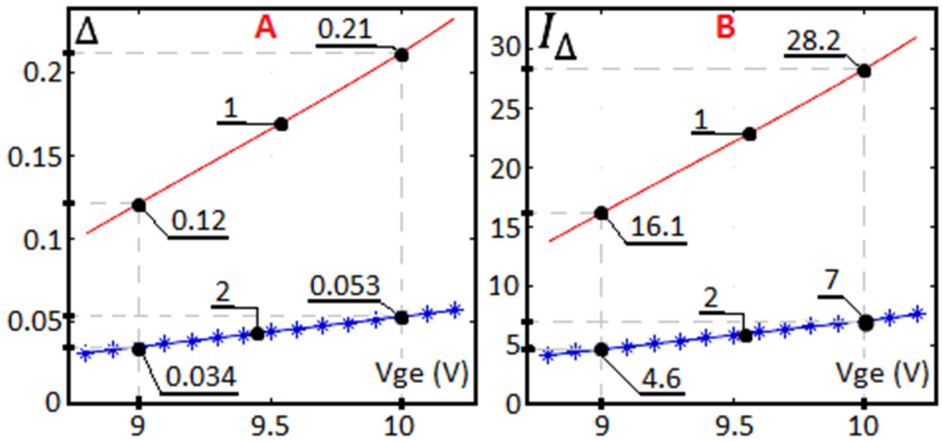


Figure 5. (**A**) Expected variation in the derating factor; (**B**) expected variation in the maximum current through the paralleled transistors. Graphics 1 and 2 at maximum and minimum thermal difference.

Step 4. Analysis of the single IGBT transistor parameters and the relevant selection requirements.

After the expected current through each transistor in parallel is found from the presented equations above with the necessary safety margin, the transistors can be selected according to several considerations about their basic parameters.

The continuous collector current through a single transistor must be considered according to the expected junction temperature as:

$$I_C = \frac{(T_{j\ max} - T_C)}{V_{CE} \times R_{th(J-C)}} \tag{11}$$

where $T_{j\ max}$ is the maximum junction temperature; T_C is the case temperature; V_{CE} is the collector-emitter saturation voltage at I_C; $R_{th(J-C)}$ is the junction-case thermal resistance of the transistor.

The peak collector current should be selected to be at least two times the nominal collector current for 1 ms at the maximum temperature.

$$I_{PK} = 2 \times I_C \tag{12}$$

The maximum dissipated power from a single IGBT transistor can be calculated from:

$$P_{\max IGBT} = \frac{(T_{j\ max} - T_C)}{R_{th(J-C)}} \tag{13}$$

As the analysed inverter naturally operates with ZVS and, hence, low switching losses, the selected transistors according to the necessary collector current and collector-emitter voltage usually cause an overrating in the power dissipation. This explains the relatively small-size heatsinks combined with forced convection, shown in the next part.

The switching losses during the transistors ON and OFF time depend on the amount of energy, respectively, E_{on} and E_{off}. The analysis can be conducted according to the following equations:

$$E_{on} = \int_{T_{on1}}^{T_{on2}} V_{CE}(t) \times I_C(t)\, dt \tag{14}$$

$$E_{off} = \int_{T_{off1}}^{T_{off2}} V_{CE}(t) \times I_C(t)\, dt \tag{15}$$

where the times T_{on1}, T_{on2}, T_{off1}, T_{off2} are, respectively, the beginning and the end of the ON and OFF periods.

As the converter operates with ZVS, the V_{CE} voltages during the ON and OFF switching will be comparable with the threshold V_{GE}, and the times $T_{on2} - T_{on1}$ and $T_{off2} - T_{off1}$ are under 100 ns, confirmed experimentally in the next part. With this, the expected switching losses can be neglected, and the conduction losses can be accepted as dominant. Their calculation is according to the equation:

$$P_{cond} = V_{CE} \times I_C = R_{CE} \times I_C^2 (W) \tag{16}$$

For the considered packages above, TO-247, TO-3PN, and TO-264, transistors with several tens of milliohms R_{CE} can be selected.

3. Experimental Setup

The experimental setup aimed to verify the designed inverter for induction heating based on paralleled IGBTs and the suggested methodology and to depict the current mismatch amongst the transistors experimentally. The experimental study was conducted as follows: converters were designed with 3, 4 and 5 transistors in parallel per side (Figure 1) following the presented step-by-step methodology in point 2; converters were manufactured using IGBTs listed in Table 1 Applications, using transistors from the same and different production lots; the derating factors and expected current mismatch were analysed according to the nominal current per inverter; the currents were measured through each transistor in parallel at full load during the entire melting cycle; the thermal differences were measured with an infrared camera on the heatsink surface. In addition, the layout and inductor construction improvements were implemented, leading to the minimisation of the oscillations.

Figure 6 shows an experimental model of the self-resonant converter for induction heating with its main components: 8 GIBT transistors, connected according to Figure 1; forced air cooling system with fans; resonant capacitor tank, inductor; and graphene crucible. The 4 selected transistors per side were considered according to previously presented Equations (1)–(16) with a current derating factor of 20%.

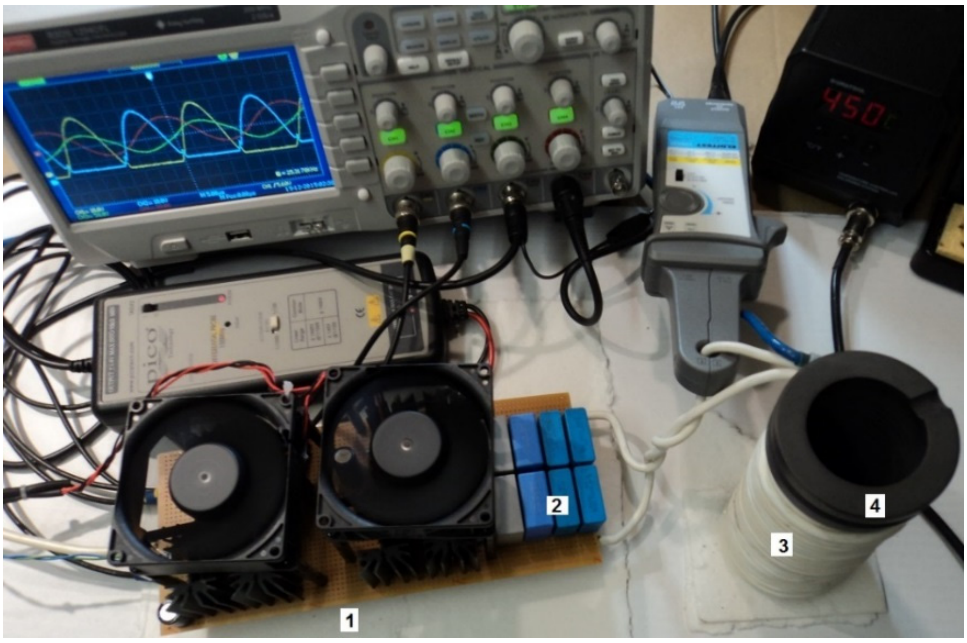


Figure 6. A model of self-resonant converter for induction heating: 1—IGBT transistors; 2—resonant capacitor tank; 3—inductor; 4—graphene crucible. The used measurement equipment is as follows: oscilloscope RS PRO RSDS1204CFL; current probe ELDITEST CP6220; voltage differential probe Pico.

The experimental study was conducted at the maximum converter power to depict the current mismatch under worst-case conditions. The results are illustrated with oscillograms, as follows:

- Figure 7. The oscillograms showed the expected current mismatch between transistors selected from the same production lot (1, 2) and transistors from two different lots (3, 4). Although all transistors were the same type, the first two conducted with a negligible difference, while transistor 3 showed a 25% higher current and transistor 4 switched on with a 540 ns delay (Figure 7A,B). The provided measurements clearly showed that a converter based on such a selection of IGBT transistors would be unreliable. In another selection, a different lot transistor (graphic 4, Figure 7C) could switch prematurely, conducting higher current, which is also an unacceptable condition.
- Figure 8. The oscillograms showed an acceptable current mismatch in the range of 2–5% at the peak point due to the layout issues and parasitic elements. The experiment was conducted in the following conditions: the transistors were selected from the same production lot; the resonant frequency during the entire heating process varied in the range 25–35 kHz, depending on the load conditions. The experimental result also confirmed the suggested current mismatch range of ±5% for the production lot. Similar results were received with the transistors shown in Table A1, Appendix A.
- Figure 9. The oscillograms presented the operation of the converter, comprised of transistors in parallel. The experiment showed a stable process in the entire frequency and power range. According to Figure 9B, the sinusoidal voltage over the inductor crossed the zero point between both sides of the voltage precisely, which experimentally proved the inverter's ability to operate in ZVS with correctly selected paralleled transistors.
- Figure 10. The proposed inverter improved from the first unit (Figure 6) by moving the capacitor tank allocated in parallel to each transistor. Although the converter layout was not an object of this research, such a layout matched better the paralleled transistors as a current mismatch amongst the IGBTs under 2% was observed.
- Figure 11. The presented thermal images provided an experimental measurement of the temperature on the heatsinks' surface. Typically, the paralleled transistors have to be assembled on a typical heat sink, sharing and equalising the temperature. In this experiment, they were intestinally separated for the thermal difference to be better depicted. The investigation showed a thermal difference between transistors in parallel with low current differences (Figure 11A,C) according to Figure 8 and high current differences (Figure 11B,D) according to Figure 7B,C.
- Figure 12. The thermal differences depicted as infrared pictures in Figure 11 are described as transient processes in an operation cycle. As Figure 12A shows, the thermal difference between transistors the Q1 and Q4 heatsink surface (Figure 7A) could reach 10 °C. The same experiment showed that the temperature difference under the worst-case conditions between transistors of the same production lot Q1 and Q2 (Figure 7A) could be minimised to 3–4 °C.
- Figure 13. The crucible reached 500 °C for 10 min; enough for melting tin with a high energy efficiency. Potentially, the entire system can be designed for higher temperatures to melt other metals, requiring higher power and, hence, powerful transistors. The system was tested with several melting cycles, giving the established transistors and crucible temperatures without overheating.
- Figure 14. The experiment showed oscillations that could potentially occur due to PCB layout issues in inverters with paralleled transistors. Usually, such oscillations occur in the gate drive circuit when transistors share the same gate drivers as the research in [51–53]. However, in this case, each transistor was controlled by an individual driver (Figure 1), and it was found that the problem originates from the conductors' length and parasitics, which occur between the PCB and the inductor.
- Figure 15 Although the above-described problems are beyond the scope of this research, a layout modification was suggested and used for all presented experimental tests. According to the circuit in Figure 15, the air-cooled inductor was divided into a

number equal to the number of paralleled transistors sections. With this, the inductors L1, L3, L5 and L7 from the high side and L2, L4, L6 and L8 from the low side correspond to inductors L1 and L2 from Figure 1. Capacitors C1-C4, in summary, represent capacitor C1 from the resonant tangent in Figure 1. Although the effect of parasitics minimisation was experimentally observed, giving the inverter's stable operation, this part requires future research and improvements.

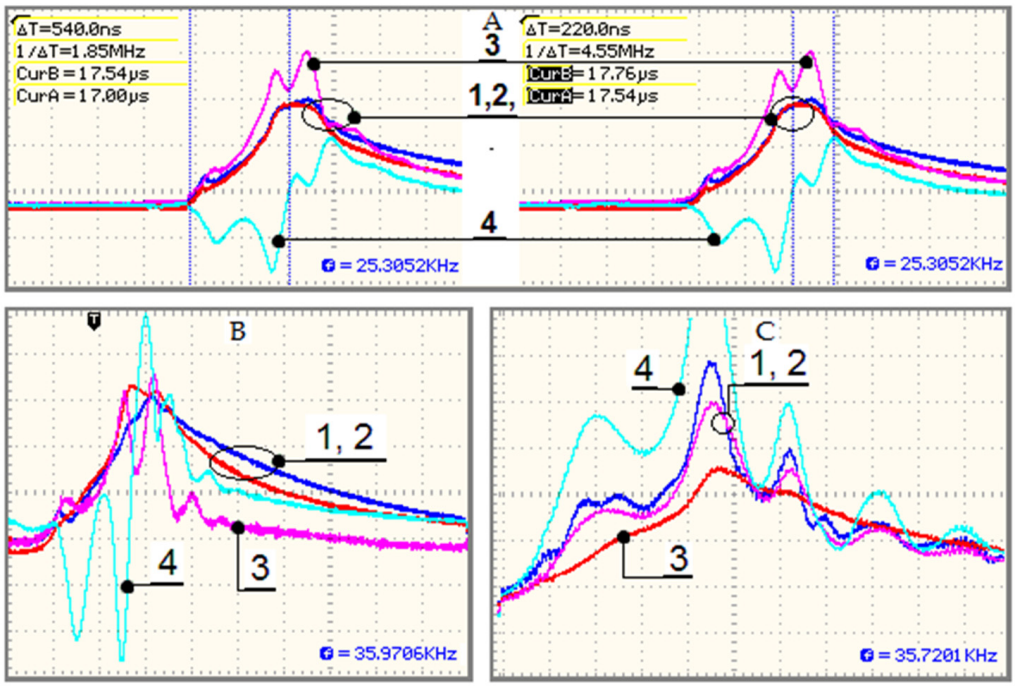


Figure 7. Current mismatch amongst four paralleled IGBT transistors. (**A**,**B**) switched-on with a delay of transistor 4; (**C**) switched-on prematurely of transistor 4; 1, 2—transistors with the same production lot; 3, 4—two different production lots.

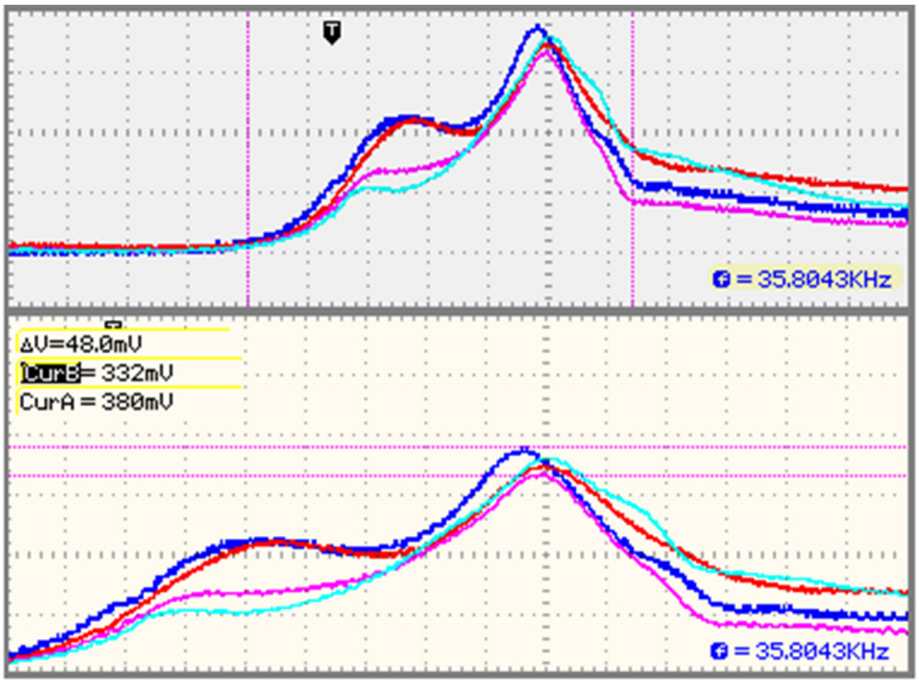


Figure 8. Minimum current mismatch amongst four IGBT transistors from the same production lot.

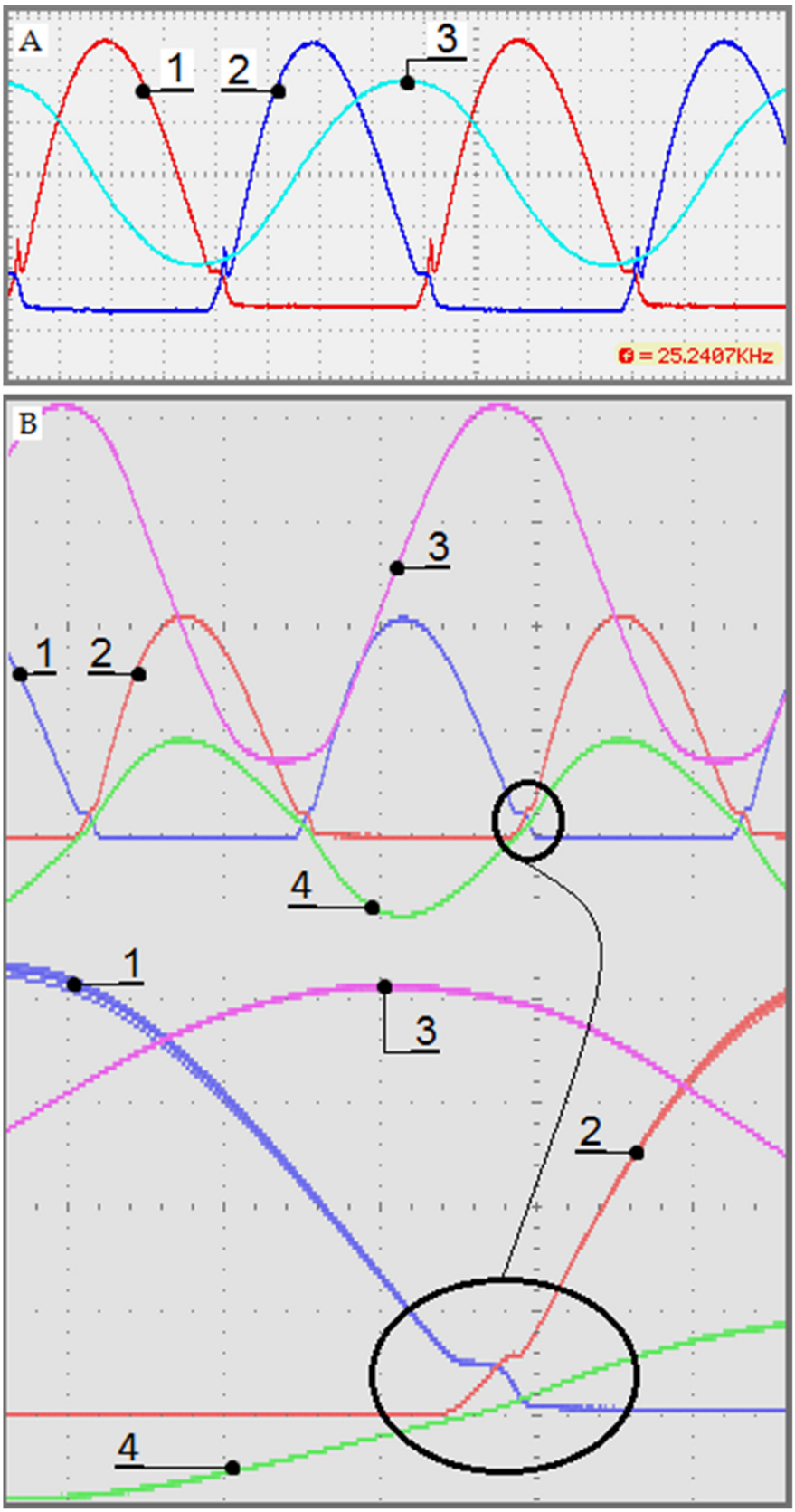


Figure 9. Operation of the inverter for induction heating. (**A**,**B**) 1, 2—voltages, respectively, over the paralleled high side (Q1, Q3, Q5, Q7—Figure 1) and low side (Q2, Q4, Q6, Q8—Figure 1) transistors; 3—current through the inductor; (**B**): 4—voltage crossing the zero switching point.

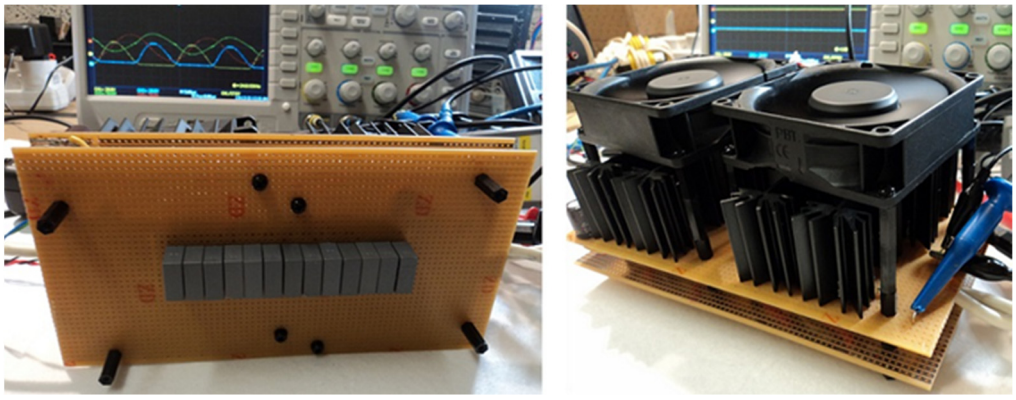


Figure 10. Improving the converter construction, given in Figure 6.

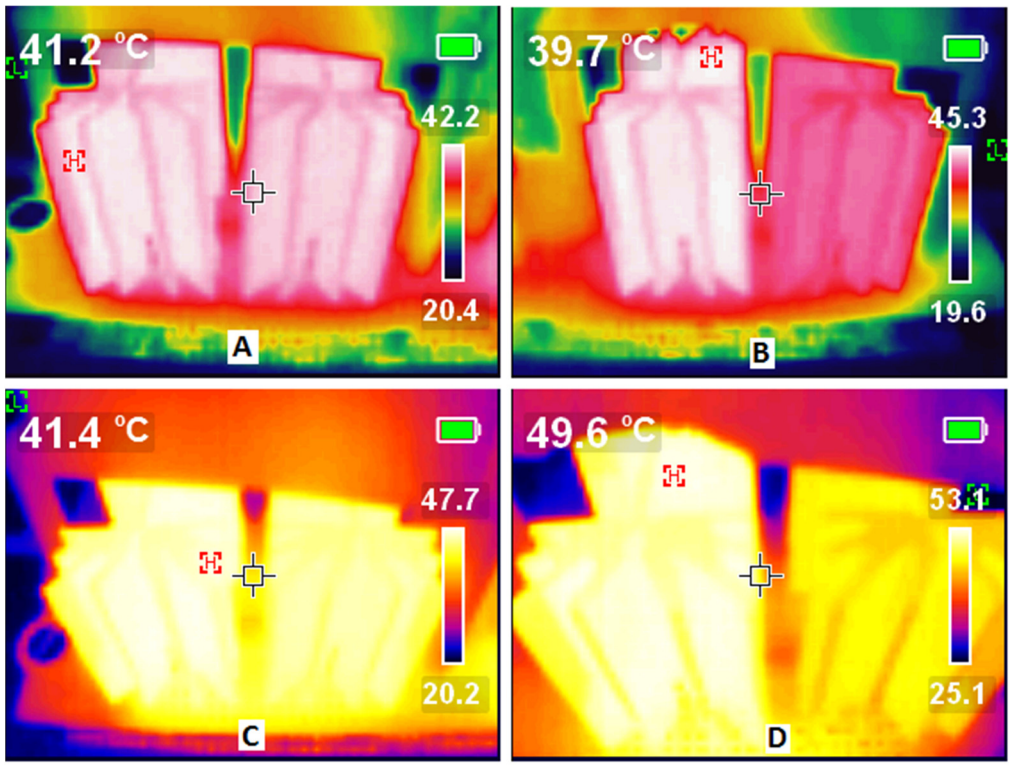
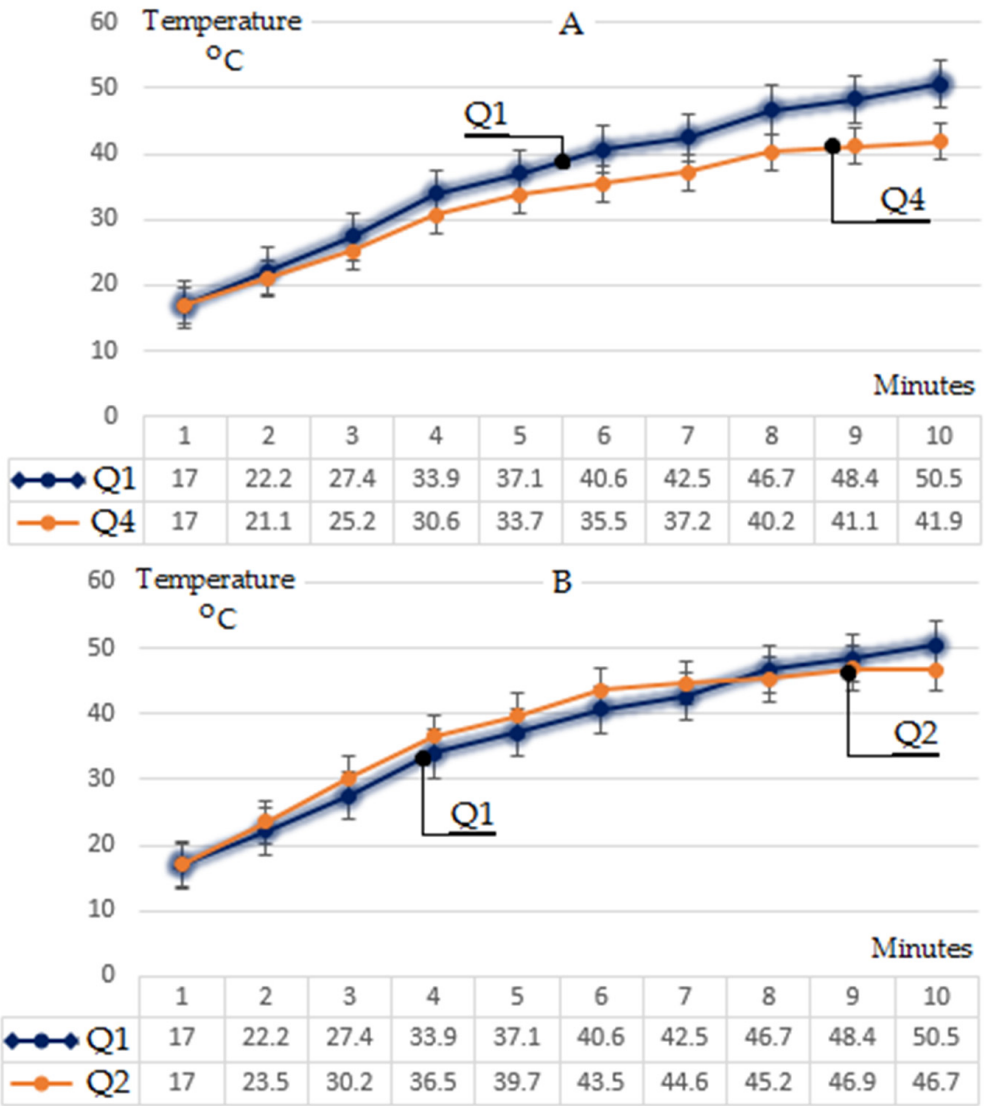


Figure 11. Infrared temperature measurements on the surface of the heatsink. (**A**,**C**) Appropriately selected transistors from the same production lot (Figure 7, graphics 1, 2); (**B**,**D**) transistors from different production lots (Figure 7 graphics 1, 4). The thermal measurements were performed with the infrared camera FLIR.



	1	2	3	4	5	6	7	8	9	10
Q1	17	22.2	27.4	33.9	37.1	40.6	42.5	46.7	48.4	50.5
Q4	17	21.1	25.2	30.6	33.7	35.5	37.2	40.2	41.1	41.9

	1	2	3	4	5	6	7	8	9	10
Q1	17	22.2	27.4	33.9	37.1	40.6	42.5	46.7	48.4	50.5
Q2	17	23.5	30.2	36.5	39.7	43.5	44.6	45.2	46.9	46.7

Figure 12. Transistors thermal difference for one melting cycle of 10 min. (**A**) Between transistors Q1 and Q4; (**B**) between transistors Q1 and Q2, both selected according to Figure 7A.

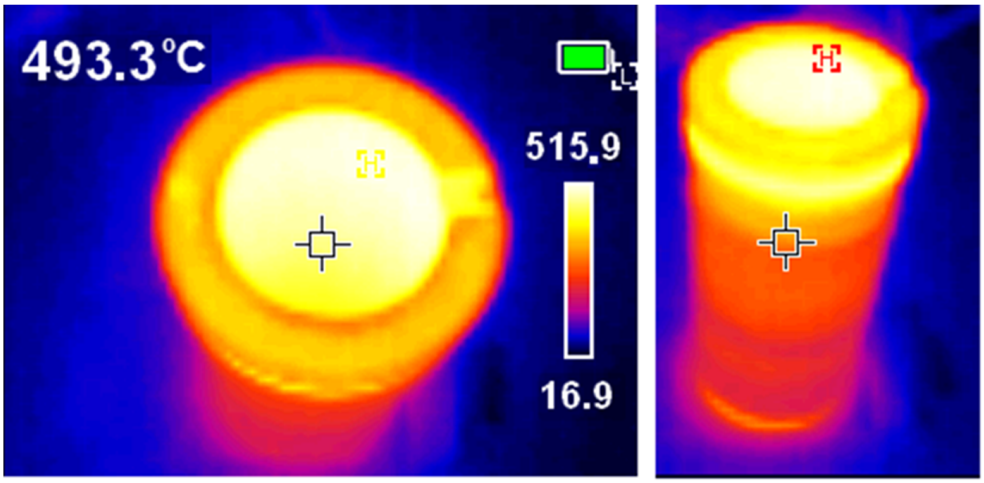


Figure 13. Infrared image of the graphene crucible, given in Figure 6.

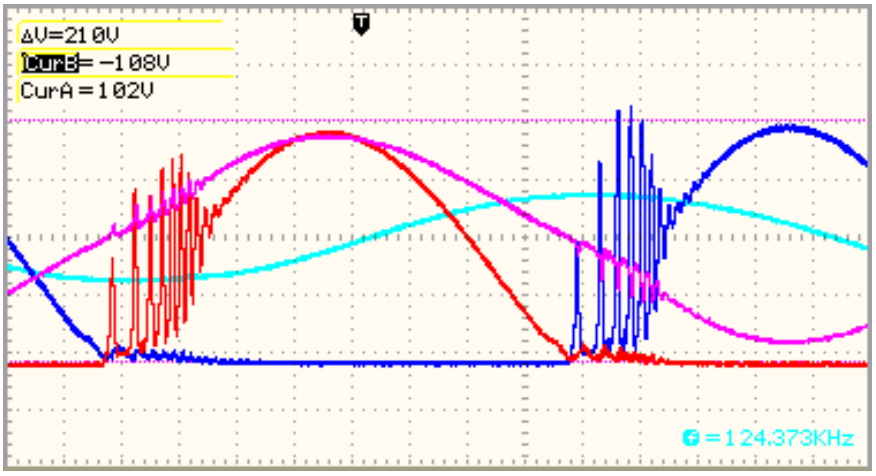


Figure 14. Oscillations due to PCB layout issues.

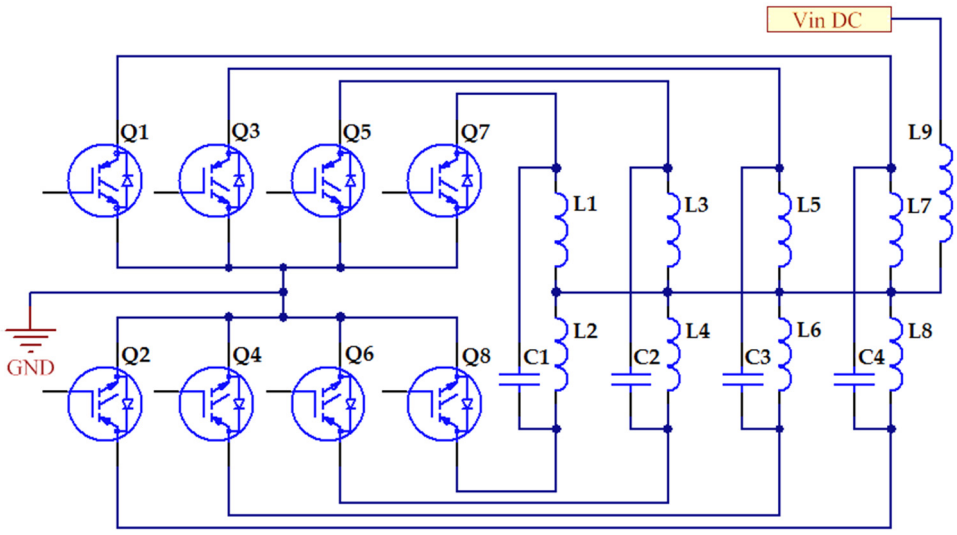


Figure 15. A suggested structure of connection.

4. Discussion

The provided experimental verification was performed with a resonant inverter for induction heating (Figure 6). As the main contribution in this research, the result showed that such a topology (Figure 1) can be completed with paralleled IGBTs, operating with low mismatch current and acceptable current difference amongst the transistors, which is supported by the presented oscillograms (Figures 7–9). The achieved current sharing amongst the paralleled IGBTs makes the ZVS mode of operation possible for a resonant inverter with paralleled transistors, which is the main advantage of the investigated topology. The presented results showed the feasibility of the investigated topology for improving the installed power of the self-resonant inverters for induction heating. As it was experimentally shown that the installed capacity can reach more than 30 kW with four IGBTs in parallel per side of the topology, it can be concluded that such a modification is applicable for small laboratory or industrial induction crucible furnaces.

The suggested methodology for analysing the paralleled IGBT transistors is based on stipulated conditions in which the transistors' static and dynamic parameters (Figure 3) are digitalised into polynomial Equations (3)–(8). The calculating procedure shows the expected parameters dispersion in a production lot (Figure 4). As a result, the necessary derating factor, the current mismatch, and the current difference amongst the paralleled transistors can be suggested (Figure 5). With this, the number of the necessary transistors in parallel can be calculated on the design level for the given application.

The temperature difference between the paralleled IGBTs, which results from the current mismatch, was in an acceptable range of several degrees Celsius. This final experiment verified the applicability of the suggested topology.

5. Conclusions

In this study, a methodology of the IGBTs' parallel work estimation and its application in the design procedure of a self-resonant inverter for a crucible induction system was demonstrated. The presented step-by-step approach showed satisfactory results, giving the required derating factors and current mismatch between the transistors.

The investigated self-resonant converter based on paralleled transistors was applied to an induction crucible melting system. It was shown that the presented circuit has a stable operation mode in ZVS with paralleled transistors. The conducted experiments showed a satisfactory current share and temperature equalisation. It can be concluded that the circuit has the magnitude to reach an installed power of 50–80 kW with several powerful modules in parallel, giving budget-friendly induction melting systems with inverters with high power density.

The suggested methodology was based on stipulated data, i.e., Equations (3)–(6) were derived only for the concrete transistor, and it did not have diverse characteristics. Despite that, such an approach for analysis is highly applicable for practical design and experimental verification.

Author Contributions: Conceptualization, B.D.; methodology, B.D., K.H., S.B., G.C.; software, B.D.; validation, B.D.; formal analysis, B.D.; investigation, B.D.; resources, G.C.; data curation, B.D., K.H., S.B.; writing—original draft preparation, B.D.; writing—review and editing, K.H., S.B.; visualization, B.D.; supervision, G.C., K.H.; project administration, G.C.; funding acquisition, N/A. All authors have read and agreed to the published version of the manuscript.

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Appendix A

Table A1. IGBT transistors, suitable for experimental verification with resonant inverters for induction heating, operating with PTC.

IGBT Transistor	Package	$I_{C(25^\circ C)}$ (A)	V_{CE} (V)	$P_{W(25^\circ C)}$ (W)	$V_{GE(th)}$/ $V_{CE(sat)}$ (V)
		$I_{C(25^\circ C)}$ =30–60 A			
RGT60TS65D	TO-247N	55	650	194	7.0/2.1
DGTD120T25S1PT	TO-247	50	1200	348	7.0/2.4
FGA50N100BNTD	TO-3P	50	1000	156	7.0/1.8
RGW00TS65D	TO-247N	50	650	254	7.0/1.9
		$I_{C(25^\circ C)}$ =60–80 A			
NGTB40N120FL2	TO-264 3L	70	1200	368	2.6/3.7
STGW39NC60VD	TO-247	70	600	250	5.75/2.4
IXA45IF1200HB	TO-247	78	1200	325	6.5/2.1
STGW40H65FB	TO-3PF	80	650	283	6.0/2.0
		$I_{C(25^\circ C)}$ =80–120 A			
FGA60N60UFD	TO-3P	120	600	298	6.5/2.4
FGA60N65SMD	TO-3PN	120	650	600	6.0/2.5
NGTB50N120FL2	TO-247	100	1200	535	6.5/2.4
IRGP6690DPbF	TO-247AD	140	600	483	6.5/1.95

Listing A1. Calculating the collector-emitter current (Ic) with polyval function in MATLAB:

```
clear
format short
Ic_max_hightemp = [0.0096; −0.106; −3.8721; 86.988; −600.32; 1365.2];
Vge = 9;                                        % Vge = 9 V
polyval (Ic_max_hightemp, Vge)                  % ans = 56.99 A
```

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