Low input-resistance low-power Transimpedance Amplifier design for biomedical applications.

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Abstract

This paper introduces a Transimpedance Amplifier (TIA) design capable of producing an incremental input resistance in the ohmic range, for input signals in the microampere range, such as are encountered in the design of instrumentation for electrochemical ampero-metric sensors, optical-sensing and current-mode circuits. This low input-resistance is achieved using an input stage incorporating negative feedback. In a Cadence simulation of an exemplary design using a 180nm CMOS process and operating with ±1.8V supply rails, the input resistance is 1.05ohms and the power dissipation is 93.6μW. The bandwidth, for a gain of 100dBohm, exceeded 9MHz. For a 1μA, 1MHz sinusoidal input signal the Total Harmonic Distortion, with this gain, is less than 1%. The input referred noise current with zero photodiode capacitance is 2.09pA/√Hz and with a photodiode capacitance of 2pF is 8.52pA/√Hz. Graphical data is presented to show the effect of a photodiode capacitance varying from 0.5pF to 2pF, when the TIA is used in optical sensing. In summary, the required very low input resistance, at a low input current level (μA) is achieved and furthermore a Table is included comparing the characteristics and a widely used Figure of Merit (FOM) for the proposed TIA and similar published low-power TIAs. It is apparent from the Table that the FOM of the proposed TIA is better than the FOMs of the other TIAs mentioned.

Keywords: Transimpedance Amplifier; Boosted Transconductance stage; Optical sensing; Low input-resistance.

1.Introduction

Biomedical systems are used in numerous health-care fields and the typical instrumentation for most biomedical systems includes optical sensors and an analog front-end. The Transimpedance Amplifier (TIA) forms an important front-end building block for these biomedical systems: see [1]-[12]. It is a current-to-voltage converter for signals in the microampere, or even sub-microampere, range. The main classifications of TIA topologies are shunt feed-back, current mode and feed-forward or open loop TIA. Low input-resistance, high gain, good linearity, low noise and sufficient band-width are some of the basic requirements for a TIA design. For accuracy, the incremental input resistance of the TIA is required to be low, i.e., in the ohmic region. A number of methods exists to achieve this [13][14][15]. One particular method that has been favoured because it offers a range of attractive features has been called a 'super-common-gate amplifier' [16] and it forms the starting point for the problem in hand for the new circuit presented in this paper.

The TIA configuration presented in this paper provides a very low input-resistance, that is achieved by incorporating a negative feedback stage to boost the transimpedance gain of the input stage. A modified long-tailed pair differential amplifier input stage that can provide a high gain forms the feedback amplifier stage in this configuration. The design also benefits from having an input that is very close to earth potential. The performance of the proposed TIA circuit is compared with previously published circuits. A unified performance metric is used for comparison purposes.

2.Circuit description and operation.

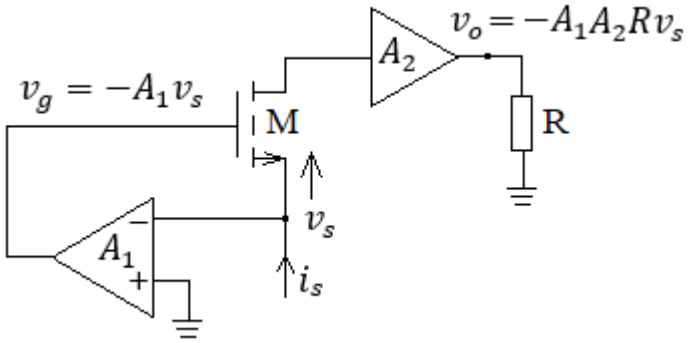

Fig.1 Schematic of the proposed TIA

Fig. 1 shows the schematic of the proposed TIA. If in Fig.1 the differential amplifier with gain-magnitude, A_1, is absent, the low frequency, small signal, input resistance looking into the source of MOSFET, M, in the common-gate configuration, is given by,

$$R_i = \frac{1}{(g_m+g_o)} \tag{1}$$

where the symbols have their conventional MOSFET meanings. A_2 represents the output stage with a current transfer ratio of unity, a low input-resistance and a high output resistance. With the amplifier, A_1 connected as shown, the incremental resistance seen looking in at the source of M is reduced because the transconductance, g_m , of M appears to be magnified by the amplifier gain. Straightforward circuit analysis gives,

$$R_i = \frac{1}{[(A_1+1)g_m+g_o]} \tag{2}$$

In the usual case $g_m \gg g_o$, so for design choice $A_1 \gg 1$, $R_i \cong \frac{1}{A_1 g_m}$

The configuration can be regarded as a `g_m-booster'. In the simplest case, A_1 is a single-stage common-source inverting amplifier for which the maximum voltage gain is the MOSFET intrinsic gain, $g_m r_o$. This increases as the drain current decreases until the

drain current reaches the logarithmic region of MOSFET operation, after which it remains sensibly constant [17]. However, it is unlikely with modern short-channel MOSFETs that the gain will exceed 100. To achieve $A_1 >> 100$ the proposed circuit uses a modified long-tailed pair differential amplifier. This arrangement also makes possible the availability of an input terminal at, or very close to, earth potential in the absence of an input signal.

A common-gate stage together with the use of negative feedback network connected between gate and source can produce a lower input resistance or a higher output resistance. We have, then, a Regulated Cascode Circuit (RGC). This is used both at the input and the output of the proposed TIA design. Fig.2 shows an N-channel MOSFET RGC.

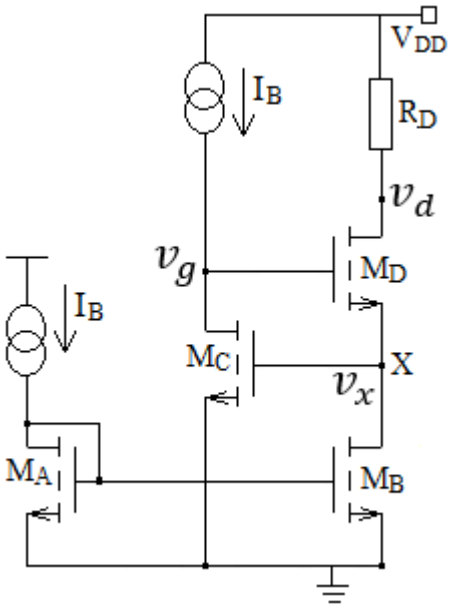

Fig.2 An N-channel RGC

Diode MOSFET M_A together with RGC MOSFET M_B comprise a simple current-mirror, supplying a bias current, I_B, to the source of output MOSFET M_D, which corresponds to M in Fig.1. M_C with its drain current load I_B, which has an incremental output resistance R_B form a single stage inverting amplifier. For the design choice $R_B \gg r_o \left(= \frac{1}{g_o}\right)$, A_1 in Fig.1 is $g_m r_o$.

Regarding the input point X, this acts at a D.C potential above earth by the gate source voltage, V_{GS} of M_C. If we require X to sit at earth then we must modify the circuit of Fig.2 by incorporating a voltage-offset scheme. The form adopted is shown, in outline, in Fig.3.

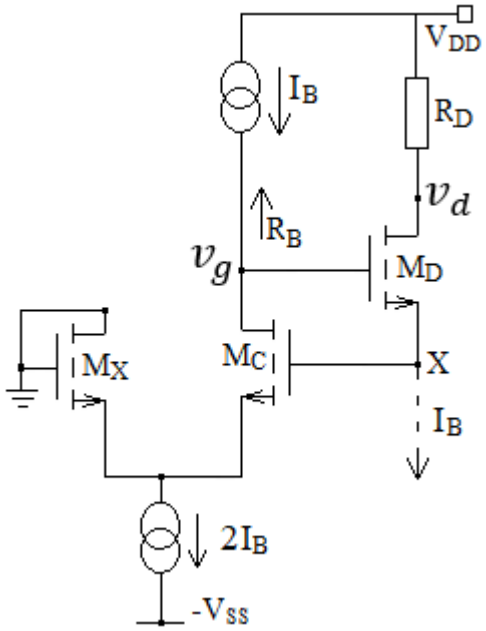

Fig.3 Input voltage-offsetting scheme

The gate-source voltages, V_{GS} of M_X matches that of M_C. So, the gate voltages of M_X and M_C is at earth potential. This arrangement means that the amplifier MOSFET M_C now has a source load resistance $\frac{1}{g_m}$, the drain source resistance of diode connected M_X, in addition to a drain load R_B, the incremental output resistance of the drain current I_B. However, provided again $R_B \gg r_o \left(\gg \frac{1}{g_m}\right)$ the stage gain is still almost $g_m r_o$.

The proposed circuit configuration in Fig.4 is an extended development of Fig.3. M_1 and M_3, with their drive currents, are the input MOSFETs of simple current-mirrors that supply bias currents for the amplifier and the bias voltages for the output stage. The input stage, corresponding to amplifier A_1 in Fig.1 is contained within the contour C. M_{10},

which corresponds to M_X, in Fig.3, is now part of a modified long-tailed pair differential amplifier input stage. The gain is enhanced by the addition of an inverter stage M_5. Feedback is provided by the source-follower M_{12} which also passes the output current.

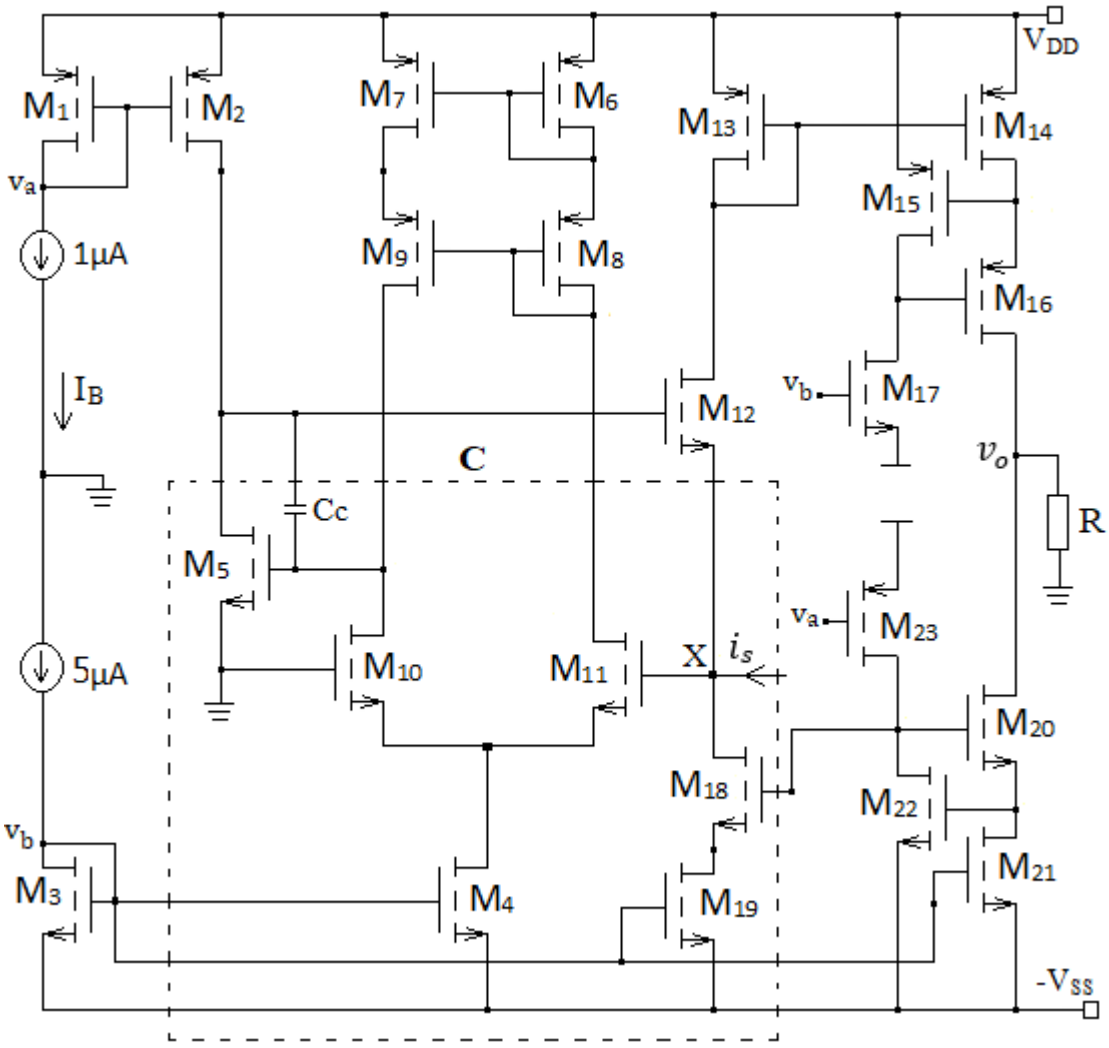

Fig.4 The proposed circuit of the TIA

The output stage corresponding to A_2 in Fig.1 comprises a P-type regulated cascode circuit (RGC) consisting of M_{14}, M_{15}, M_{16} driving an N-type RGC consisting of M_{20}, M_{21}, M_{22}. The amplifier MOSFETs M_{15} and M_{22}, respectively, of these RGCs are supplied by drain current loads provided by M_{17} and M_{23}, which are the output stages of current mirrors. Their purpose is to improve the amplifier gains provided by M_{15} and M_{22} and

thus maximise the output resistances of the RGCs.

We start the analysis by calculating the magnitude of the low frequency amplifier loop-gain in order to determine the amplifier input-resistance, then find the loop-gain frequency-dependence to investigate feedback stability, taking into account the possible use of a photodiode.

Assume the input current i_s is zero and imagine the feed-back loop is cut between the drain of M_5 and the gate of M_{12}, without disturbing the D.C conditions, and that a small voltage test signal v_t is applied to the gate of M_{12}. Hence,

$$v_{g12} = v_t. \tag{3}$$

in which the subscript number following the terminal indicated refers to MOSFET number. The source-follower voltage gain of M_{12} is $G = \frac{g_{m12}R_x}{1+(g_{m12}R_x)}$, where, R_x is the resistance seen at the source of M_{12}.

Hence, $v_{g11} = Gv_t$ (4)

The amplifier action, taking into account the current-mirror connection between the drain loads of M_{10} and M_{11}, gives

$$v_{d10} = g_{m(10,11)}R_S G v_t \tag{5}$$

where, $R_s = r_{o9}||r_{o10}$. Following further amplification,

$$v_{d5} = -g_{m5}R_D v_{d10} \tag{6}$$

where, $R_D = r_{o5}||r_{o2}$

Hence, the magnitude of the loop-gain is,

$$|L.G| = \left|\frac{v_{d5}}{v_{g12}}\right| = g_{m5}R_D g_{m(10,11)}R_S G \tag{7}$$

Thus, from eqns. (2) and (7) amplifier input resistance R_i , is given by

$$R_i \cong \frac{1}{(g_{m5}R_D g_{m(10,11)}R_S G)g_{m12}} \tag{8}$$

Comparing eqn. (8) with (1) the input-resistance is decreased by a factor

$g_{m5}R_D g_{m(10,11)}R_S G$.

When it comes to finding the dominant pole in the frequency response of the loop-gain, Fig.5 is applicable. Circuit complexity suggests the use of `Open Circuit Time Constant Analysis' [18]. In this the equivalent time constant associated with each capacitor in the signal path is found with all the others regarded as open circuits. If these add up to τ_T then the angular frequency ω_d of the dominant pole is $\omega_d = \frac{1}{\tau_T}$.

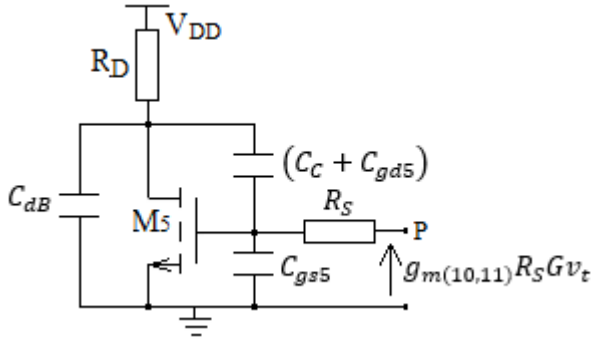

Fig.5 Circuit for analysis of M_5 frequency response

It works out that,

$$\tau_T = [R_D + R_S(1 + g_{m5}R_D)](C_{gd5} + C_c) + R_S\left[(C_{gs5} + C_c) + C_{dB}\right] + R_D C_{db} + R_i C_{PD} \quad (9)$$

The first term in the R.H.S of (9) involves the Miller Effect and it dominates in determining τ_T, if we choose the stabilization capacitor C_C to be in the pF range. All other capacitances, except photodiode junction capacitance, C_{PD} , are in the femtofarad range and R_i is very small compared with R_D and R_S. The circuit of Fig.5 is analysed rigorously in [19] and it is shown that the τ_T of eqn. (9), without the term $R_i C_{PD}$ (which is not applicable in its analysis) is the same.

3.Results and Discussion.

The proposed TIA circuit in Fig. 4, was simulated in Cadence using TSMC 180nm CMOS process technology with power supplies V_{DD} = -V_{SS} = 1.8V. The MOSFET dimension data are as shown in Table 1. The total power dissipation is 93.6µW.

Table 1: MOSFET dimensions

MOSFET	M_4	M_{17}	All other MOSFETs
W/L (µm)	0.18/0.36	9/0.36	1.8/0.36

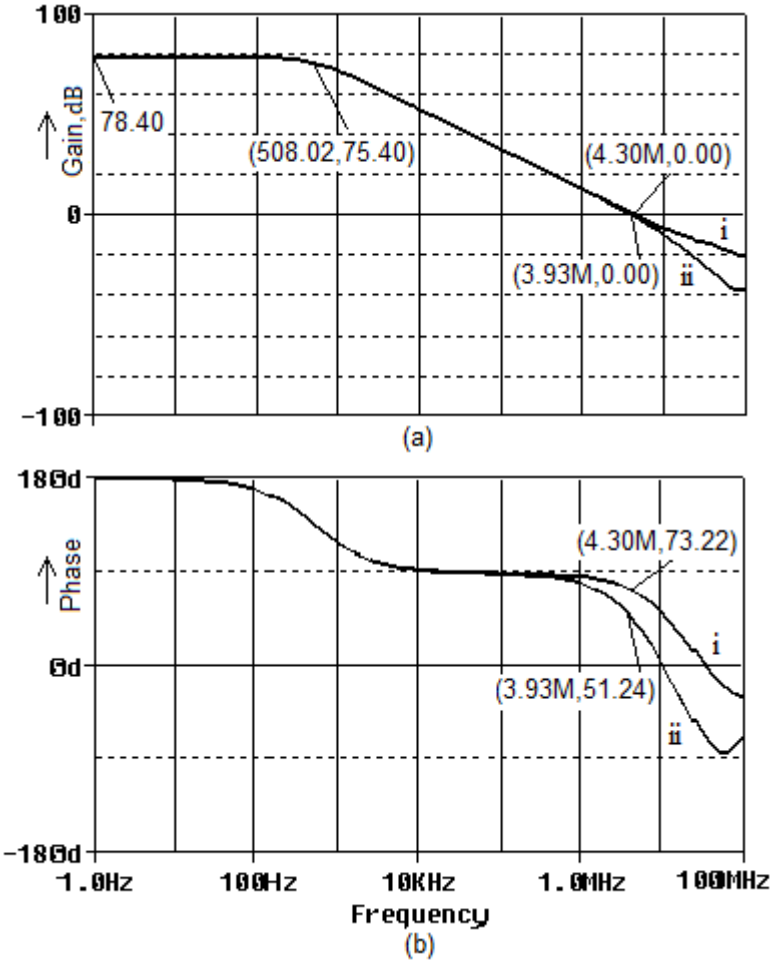

Fig.6 Bode Plots of Open-Loop gain and Phase margin of the Amplifier Section of the proposed TIA

Fig. 6 shows the Bode plots of Open-Loop Gain (L.G) and Phase of the amplifier section of Fig.4 (the section within contour C) for the proposed TIA. From the magnitude plot: (i) for C_{PD} = 0, (ii) for C_{PD} = 2pF, the |L. G|=78.40dB. This corresponds to a numerical value of 8326V/V. In the Bode phase plot of Fig.6(b) the phase margin is 73˚ for (i) C_{PD} = 0 and 51˚ for (ii) C_{PD} = 2pF (approx.). An acceptable Phase Margin of 51˚ guarantees loop stability, when a photodiode with a junction capacitance of 2pF is used.

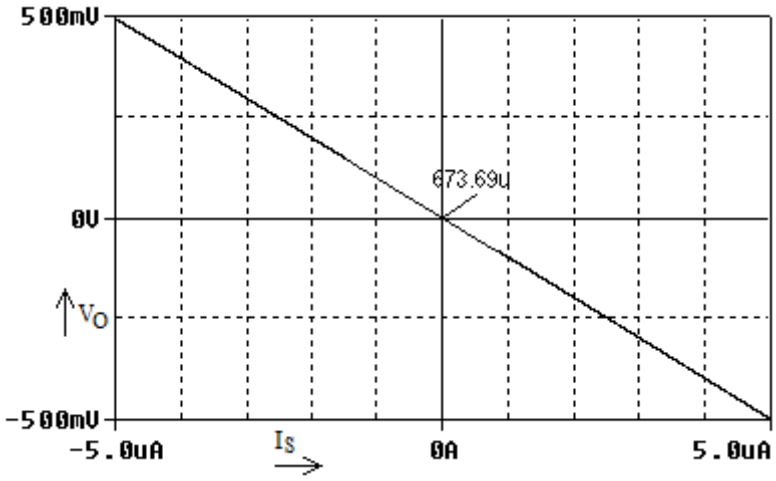

Fig.7 D.C characteristic with a load resistance R=100kΩ

Fig.7 shows the DC transfer characteristic (V_O versus I_S) for R=100kΩ corresponding to a TIA nominal gain of 100dBΩ. It appears to be linear and pass through the origin but there is actually a small voltage offset that is attributed to a mismatch between the D.C output characteristics of the N and P channel RGCs in the output stage. The direction of the slope is indicative of signal inversion. Thus, referring to Fig.4, $I_{D12} = I_{D18} - I_{D5}$. So, if $I_{D5} > 0$ then I_{D12} decreases as does I_{D13} with the result that $V_O < 0$. The magnitude of the slope defines the gain. On the scales used this appears to be in agreement with design value.

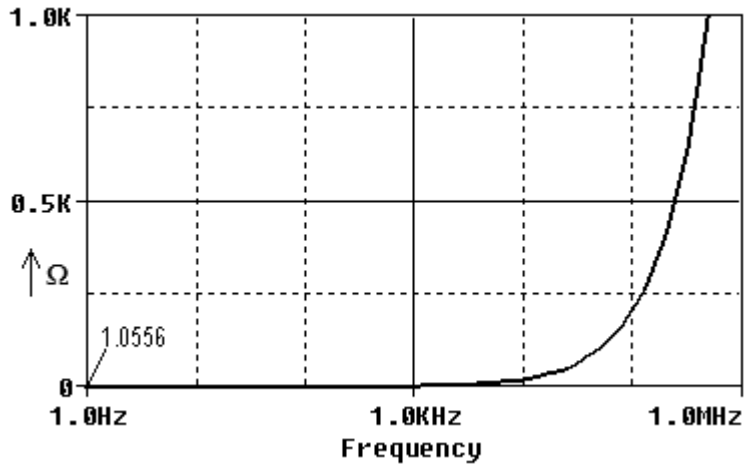

Fig.8 Input impedance, of the proposed TIA

Fig. 8 is self-explanatory: the input impedance Z_i is purely resistive at low frequencies; thus $Z_i(0) = R_i = 1.05\Omega$. The calculated input resistance based on process data for g_m and measured L.G is, 1.02Ω, which is in good agreement with the measured one. Z_i increases with frequency and becomes inductive. The measured output resistance, 177.9MΩ, is designed to be high, via the use of RGCs in the output stage, in order to be at least a decade higher than any load resistance, R, likely to be used.

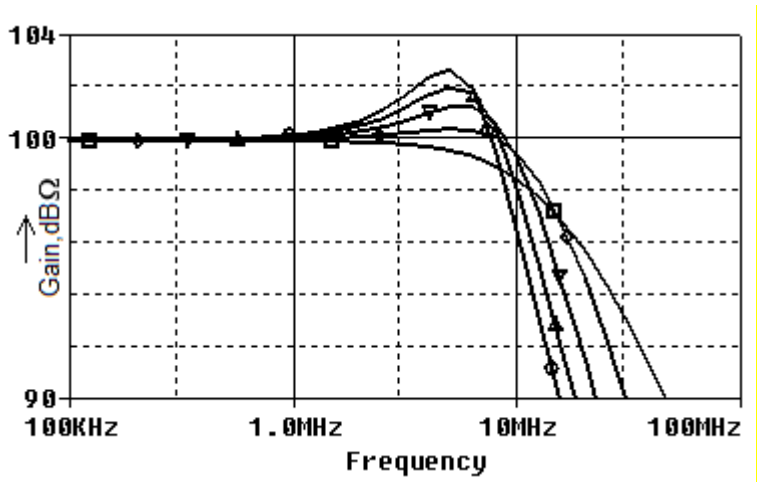

Fig.9 TIA gain magnitude plots with a load capacitance of 0.1pF. The curves with symbols □ ◇ ▽ △ ○ correspond, respectively, to curves for C_{PD} (pF) = 0, 0.5,1,1.5,2

Furthermore, for the values of C_{PD} shown in Fig.9, the -3dB bandwidths of the TIA are respectively 15.44MHz, 15.27MHz, 12.74MHz, 10.88MHz and 9.61MHz with a TIA gain of 99.93dBΩ. The TIA gain magnitude departs by a small amount from the design value of 100dBΩ because the output impedance is non-infinite. With C_{PD} = 0pF there is no overshoot and with increasing value of C_{PD} the overshoot is due to the decrease in phase margin in the amplifier. The maximum overshoot is for C_{PD} =2pF. For C_{PD} = 0pF the phase margin is 73˚ and for C_{PD} = 2pF the phase margin is 51˚ as shown in Fig.6b. This is thought to be a good phase margin to ensure frequency stability in the amplifier.

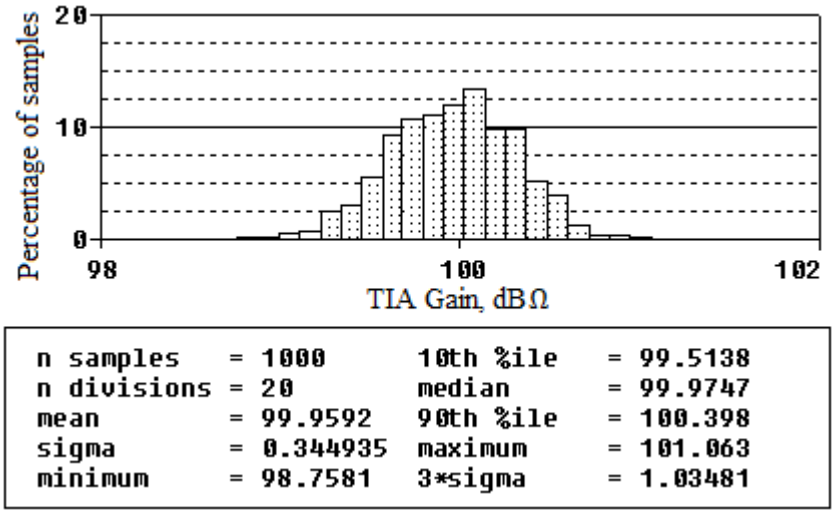

Fig. 10 Monte-Carlo simulation for the proposed TIA

The effect of process variation on the proposed TIA is shown in Fig.10 for 1000 runs using Monte-Carlo simulation. The mean value of the transimpedance gain is 99.95dBΩ with a standard deviation of 0.34dBΩ.

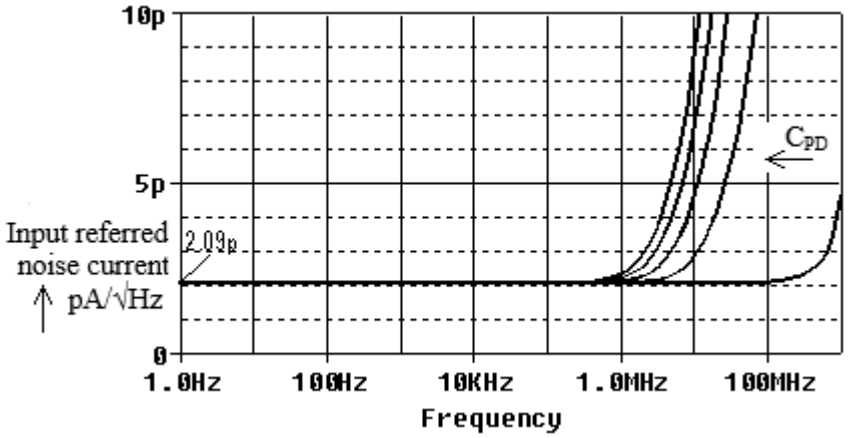

Fig.11 Input referred noise current of TIA with C_{PD} (pF) = 0, 0.5,1,1.5,2 and a capacitance of 0.1pF across R: this allows up to 100fF loading of following circuits. The arrow indicates the direction of variation of C_{PD} from 0 to 2pF

Noise in a TIA is always referred to the input to allow fair comparison between different circuit topologies. The total input referred noise current is obtained by dividing the rms output noise voltage by the TIA transimpedance value. Considering the noise contribution by each of the transistors and the resistor, it is found that the transistors M_{14} and M_{21} in the output regulated cascode stage are the main contributors to the noise. The noise characteristics of Fig.8 shows a constant value of 2.09pA/√Hz up to 100MHz when the photodiode junction capacitance is 0. The input referred noise current is 8.52pA/√Hz at -3dB frequency when C_{PD} = 2pF.

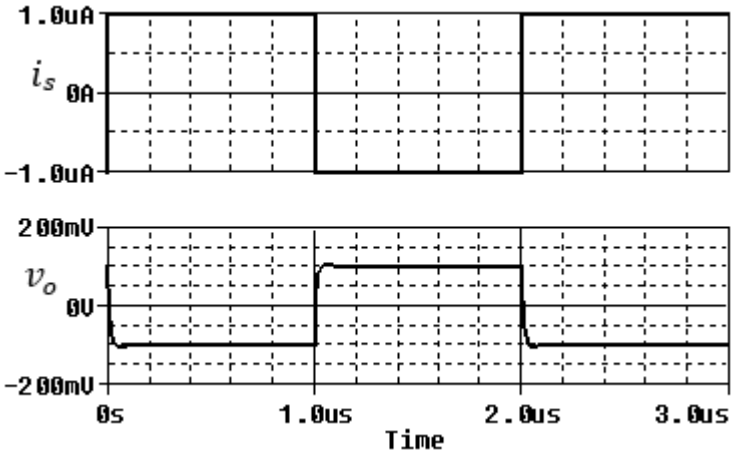

Fig.12 The upper trace shows a square wave input signal: the lower trace shows the response with $C_{PD} = 0$

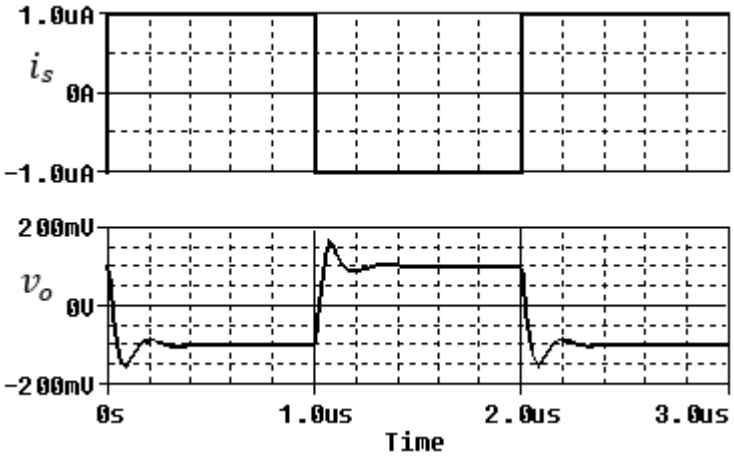

Fig.13 Output signal response to a square wave input signal with $C_{PD} = 2pF$

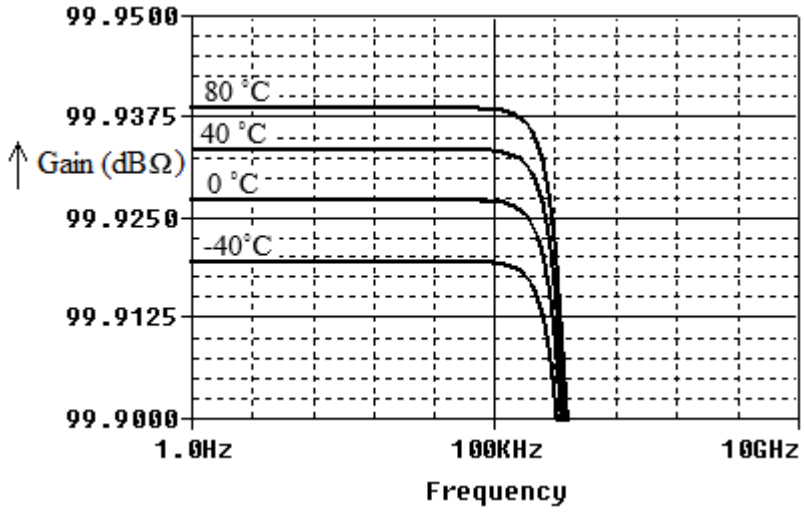

Fig.14 Effect of temperature variation on the TIA with $C_{PD} = 0$

In Fig.12 and Fig.13, the output response given, is for a gain magnitude of 100dBΩ with C_{PD} = 0 and 2pF respectively. Fig.14 shows the effect of temperature variation on the TIA gain with C_{PD} = 0.

Table 2: TIA performance comparison for References indicated.

Circuit characteristics	Proposed circuit	[20]	[21]	[22]	[23]
Transimpedance gain	99.9dBΩ	62 dBΩ	104.8 dBΩ	68.8 dBΩ	75 dBΩ
Bandwidth	9.6MHz	11GHz	50MHz	5.5GHz	5.2GHz
Input referred noise	8.52pA/√Hz	30pA/√Hz	22pA/√Hz	19pA/√Hz	6.9pA/√Hz
Power dissipation	93.6µW	66mW	0.34mW	18mW	7.15mW
Photodiode capacitance	2pF	200fF	2pF	650fF	0.075p
Process technology	180nm	65nm	130nm	180nm	40nm
FOM	7.6×10^{11}	1.3×10^{7}	3.2×10^{11}	3.8×10^{8}	6.1×10^{8}

Table 2 compares the performance of the proposed TIA with other published TIAs. The TIAs are compared based on a widely used Figure of Merit (FOM) [24] as given in eqn. (10).

$$FOM = \frac{\sqrt{BW(Hz)}R(\Omega)C_{PD}(pF)}{Noise(\frac{pA}{\sqrt{Hz}})P(mW)} \quad (10)$$

where BW is the band-width, R is the TIA gain, C_{PD} is the photodiode junction capacitance, *Noise* is the input referred noise current and P is the total power dissipation. The proposed circuit shows the best performance for a low-power TIA in terms of the FOM as shown in Table 2.

Conclusions

In this paper we have presented the Cadence simulation results of an exemplary TIA intended for biomedical use with microampere and nanoampere input signals and shown that it is possible to design a low-power TIA amplifier that has the following performance characteristics for ±1.8V power supplies: power dissipation 93.6μW; low input-resistance 1.05Ω; wide bandwidth (>9MHz with a nominal gain of 100dBΩ); at this bandwidth the input referred noise current with C_{PD} = 0 is 2.09pA/√Hz and with C_{PD} = 2pF is 8.52pA/√Hz. It is apparent from Table 2 that a widely used FOM of the proposed TIA is significantly better than that of the other low-power, low frequency, TIAs with which it is compared. Additionally, the DC input and output levels are at earth or within a few mVs of it.

Acknowledgements

The authors would like to thank the reviewers for their perceptive and valuable comments.

Data availability declaration.

Data will be made available on reasonable request.

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